FIGURE 4-1

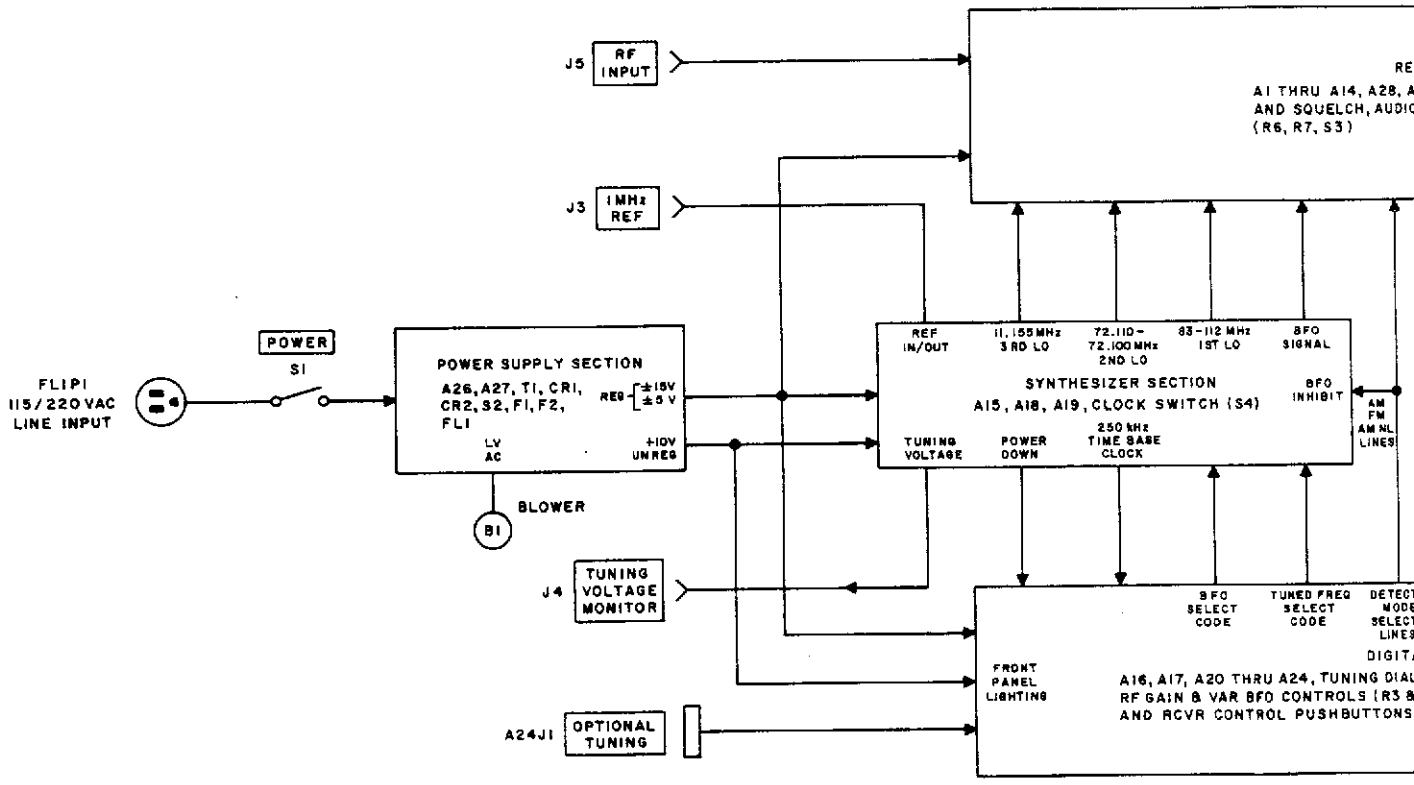


Figure 4-1. WJ-8888, Simplified Overall Block Diagram

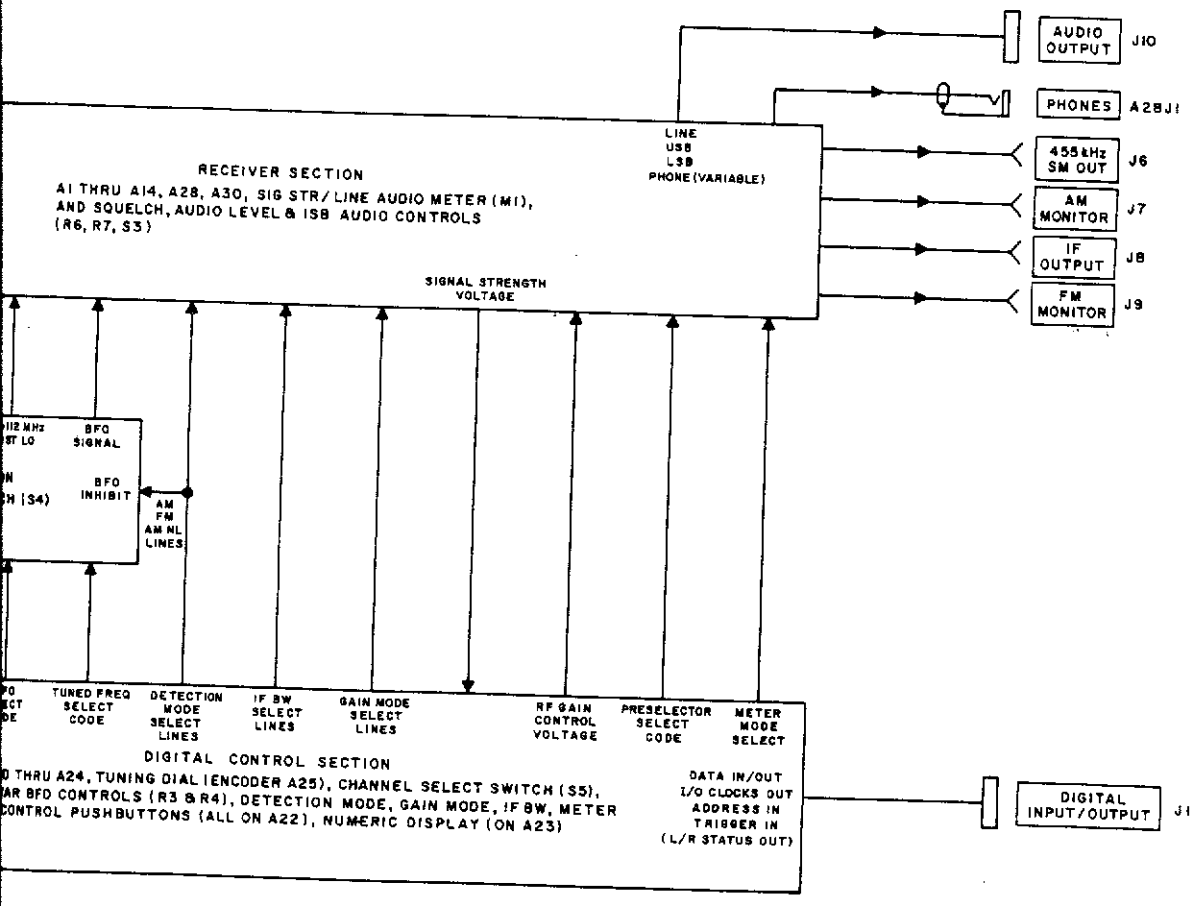

AUDIO OUTPUT
J10
PHONES
A28J1
455kHz SM OUT
J6
AM MONITOR
J7
IF OUTPUT
J8
FM MONITOR
J9
LINE
USB
LSB
PHONE (VARIABLE)
RECEIVER SECTION
A1 THRU A14, A28, A30, SIG STR/LINE AUDIO METER (M1), AND SQUELCH, AUDIO LEVEL & ISB AUDIO CONTROLS (R6, R7, S3)
SIGNAL STRENGTH VOLTAGE
BFO SIGNAL
BFO INHIBIT
AM FM AM NL LINES
TUNED FREQ SELECT CODE
DETECTION MODE SELECT LINES
IF BW SELECT LINES
GAIN MODE SELECT LINES
RF GAIN CONTROL VOLTAGE
PRESELECTOR SELECT CODE
METER MODE SELECT
DIGITAL CONTROL SECTION
A24, TUNING DIAL (ENCODER A25), CHANNEL SELECT SWITCH (S5), BFO CONTROLS (R3 & R4), DETECTION MODE, GAIN MODE, IF BW, METER CONTROL PUSHBUTTONS (ALL ON A22), NUMERIC DISPLAY (ON A23)
DATA IN/OUT
I/O CLOCKS OUT
ADDRESS IN
TRIGGER IN
(L/R STATUS OUT)
DIGITAL INPUT/OUTPUT
J1

FIGURE 4-2

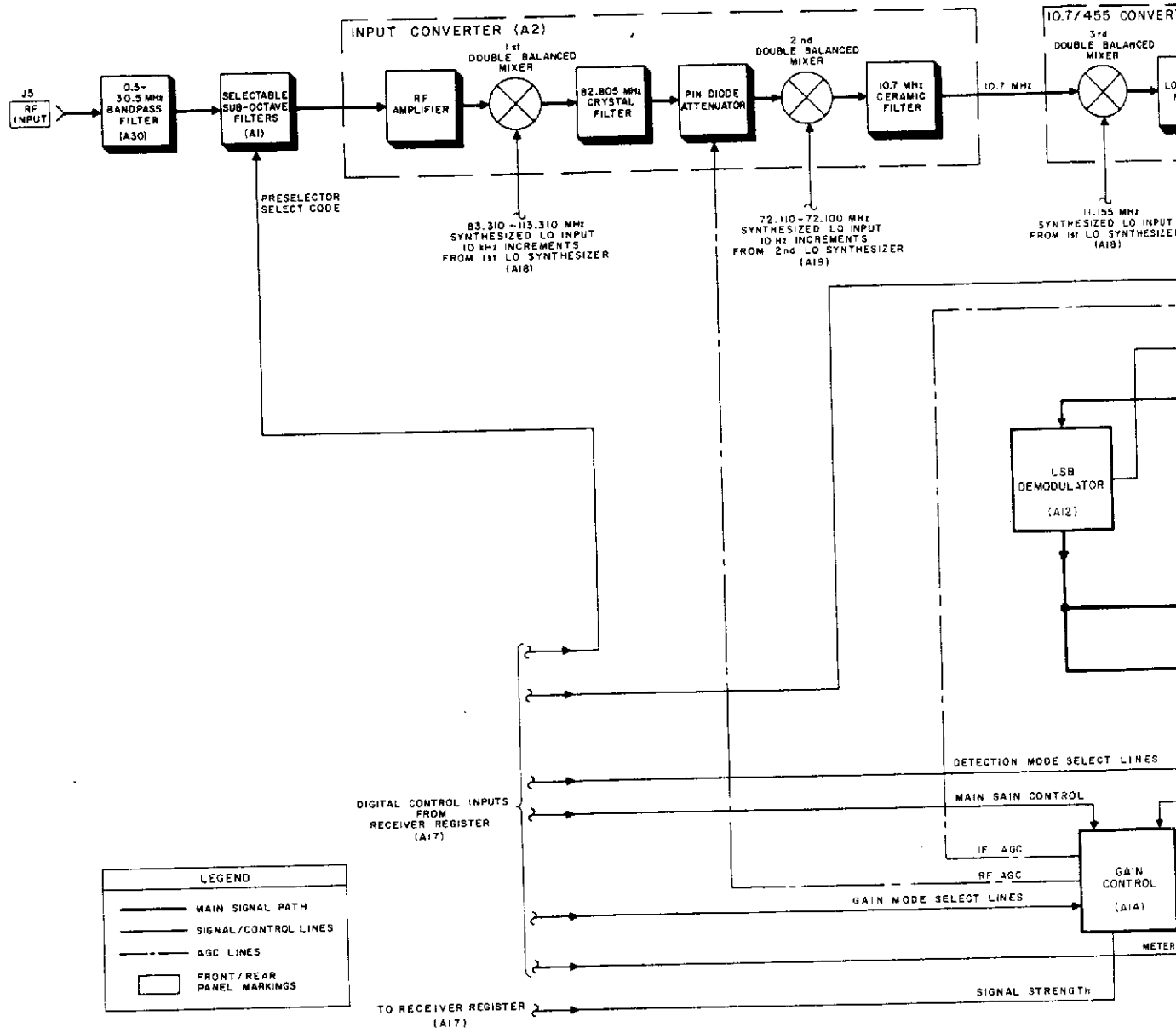
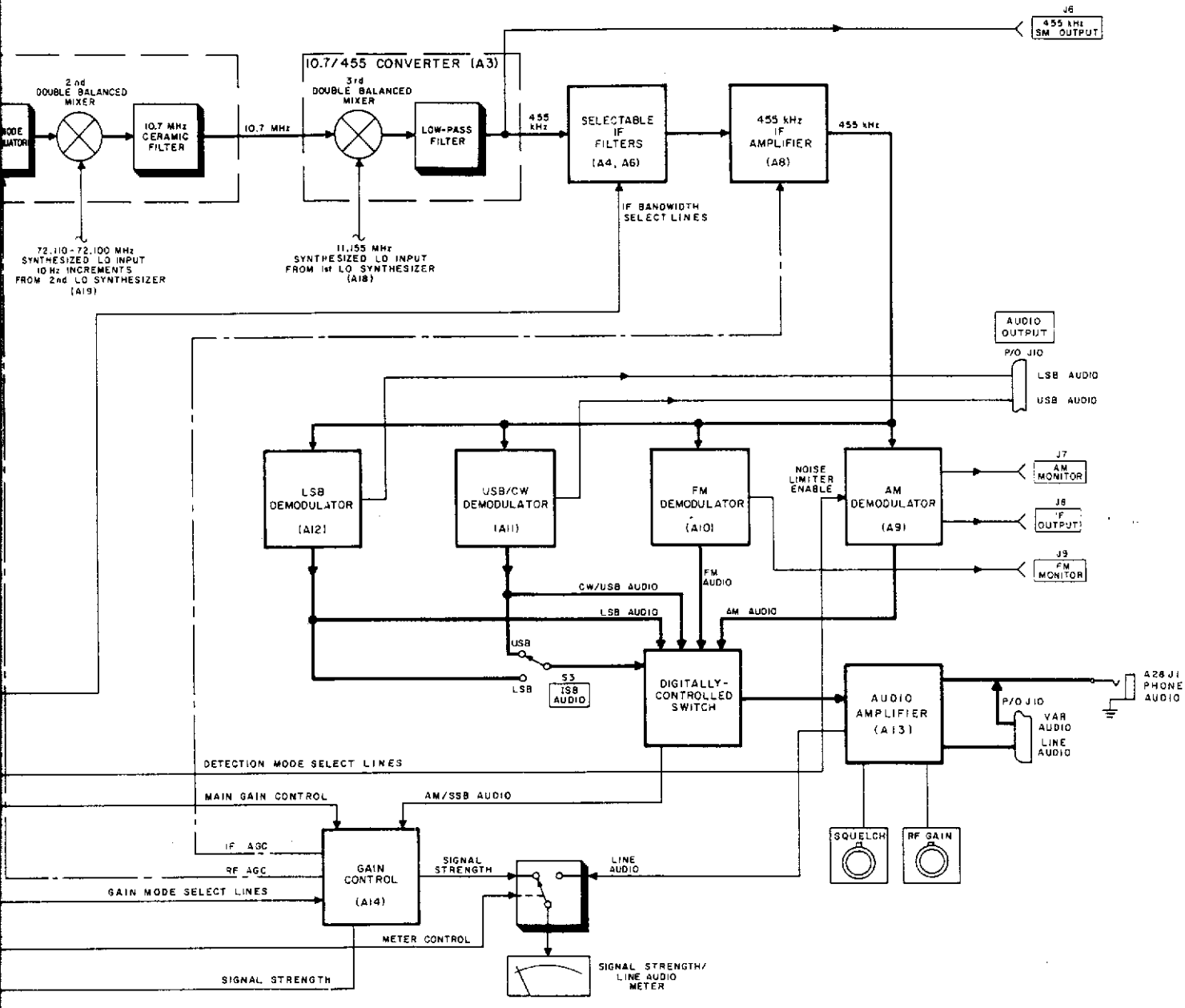


Figure 4-2. Receiver Section, Simplified Functional Block Diagram


J6
455 kHz SM OUTPUT
10.7/455 CONVERTER (A3)
2nd DOUBLE BALANCED MIXER
10.7 MHz CERAMIC FILTER
10.7 MHz
3rd DOUBLE BALANCED MIXER
LOW-PASS FILTER
455 kHz
SELECTABLE IF FILTERS (A4, A6)
455 kHz IF AMPLIFIER (A8)
455 kHz
IF BANDWIDTH SELECT LINES
72.110-72.100 MHz SYNTHESIZED LO INPUT 10 Hz INCREMENTS FROM 2nd LO SYNTHESIZER (A19)
11.155 MHz SYNTHESIZED LO INPUT FROM 1st LO SYNTHESIZER (A18)
AUDIO OUTPUT
P/O J10
LSB AUDIO
USB AUDIO
LSB DEMODULATOR (A12)
USB/CW DEMODULATOR (A11)
FM DEMODULATOR (A10)
NOISE LIMITER ENABLE
AM DEMODULATOR (A9)
J7
AM MONITOR
J8
IF OUTPUT
J9
FM MONITOR
CW/USB AUDIO
FM AUDIO
LSB AUDIO
AM AUDIO
USB
LSB
S3
ISB AUDIO
DIGITALLY-CONTROLLED SWITCH
AUDIO AMPLIFIER (A13)
A28J1
PHONE AUDIO
P/O J10
VAR AUDIO
LINE AUDIO
DETECTION MODE SELECT LINES
MAIN GAIN CONTROL
AM/SSB AUDIO
IF AGC
RF AGC
GAIN MODE SELECT LINES
GAIN CONTROL (A14)
SIGNAL STRENGTH
LINE AUDIO
SQUELCH
RF GAIN
METER CONTROL
SIGNAL STRENGTH
SIGNAL STRENGTH/ LINE AUDIO METER

SECTION IV
CIRCUIT DESCRIPTION

4.1 GENERAL

The following paragraphs describe the various circuits of the WJ-8888 Receiver. The receiver is, for purposes of description, divided into four functional sections, these being the receiver section, synthesizer section, digital control section, and the power supply section. An overall simplified functional description preceeds detailed descriptions of the four functional sections. The discussions of the receiver, synthesizer, digital control, and power supply sections consist of schematic descriptions introduced by more detailed functional discussions of these sections. Functional block diagrams are included where required. The schematic descriptions are arranged in functional sequence rather than in numerical sequence to facilitate progressive reading. The table of contents of this manual should be consulted for locating descriptions of specific circuits. It is assumed that the reader of this section is familiar with the preceeding sections of this manual.

In this instrument, the unit numbering system is used for identification of electrical components, such that each circuit-board or assembly part carries a prefix before the usual class letter and item number. For example, the full designation for R1 on circuit board A4 is A4R1. These prefixes are omitted on illustrations and in the text except where they are necessary to avoid confusion.

4.2 OVERALL FUNCTIONAL DESCRIPTION

The simplified overall diagram, Figure 4-1, shows the relationship between the four major functional sections of the WJ-8888. The blocks shown on the drawing list subassemblies and controls falling into each functional category, permitting the main chassis schematic, Figure 7-33, to be keyed to this diagram.

The receiver section tunes to a selected center frequency in the 0.5 to 30.5 MHz range from the RF input connector (antenna input). The signal may be AM, FM, pulsed CW, SSB (USB or LSB), or ISB (independent sideband). The signal is demodulated as required to produce an audio output. Wideband IF, predetection IF, and AM and FM monitor outputs are also provided by the receiver section.

Most of the operating parameters of the receiver section are controlled by the digital control section, including the tuned frequency and BFO frequency which are controlled indirectly via the synthesizer section. The specified receiver parameters controlled by the digital control section are shown on the block diagram. An analog signal strength voltage is returned from the receiver section to the digital control section where it is converted to binary code for inclusion in the data word (to be discussed in paragraph 4.5).

The tuned frequency and BFO select codes applied to the synthesizer section cause the synthesizer to provide appropriate first and second LO and BFO frequencies to the receiver section. The third LO frequency is fixed at 11.155 MHz. The BFO synthesizer output is disabled when the detection mode is AM, FM or AM NL. The proper receiver preselector is automatically selected as a

function of the tuned frequency. The digital control section obtains its time base clock from the synthesizer section. In addition, the power-down detector is located in the synthesizer section, although the main power-down latch circuit is located in the digital control section.

The specifications of the 1 MHz reference input/output, the tuning voltage monitor output, the optional tuning input, and the digital control input/output, the optional tuning output, and the digital control input/output, as well as the receiver section inputs and outputs and power requirements are described in detail in sections I and II of this manual.

4.3 RECEIVER SECTION

In this paragraph, the RF, IF, demodulation, and AF portions of the WJ-8888 Receiver are described. The discussion begins with a functional block diagram description, which is followed by a detailed circuit description based on the schematic diagrams. The circuit descriptions are arranged in functional rather than numerical sequence to facilitate progressive reading.

4.3.1 FUNCTIONAL BLOCK DIAGRAM DESCRIPTION. - Referring to functional block diagram Figure 4-2, the broadband signal from the receiving antenna is applied through J5 (RF INPUT) to a 0.5-30 MHz bandpass filter (A30). The filter output is applied to one of eight digitally selectable sub-octave filters (the term sub-octave filter refers to the fact that the passband extends over a less than 2-to-1 frequency range). Digital filter select data from the receiver register automatically selects the sub-octave filter appropriate for the frequency being tuned. The broadband nature of the input filters eliminates the need for variable-tuned RF circuitry, thus avoiding alignment and tracking difficulties. The output of the sub-octave filter is amplified by a grounded-gate JFET RF amplifier and then mixed in the first double-balanced mixer with a 83.310-113.310 MHz LO signal obtained from the synthesizer section. The 82.805 MHz difference frequency is used as the first IF.

The mixer output is applied to a crystal filter which passes only the 35 kHz-wide difference-frequency band centered at 82.805 MHz. The 82.805 MHz IF signal is applied to a PIN diode attenuator which is controlled by the RF AGC voltage derived in the gain control section. A shaper circuit provides the desired RF AGC characteristic. After attenuation, the signal is mixed with a 72.110-72.100 synthesized LO signal in the second double-balanced mixer to produce sum and difference frequencies. The 10.7 MHz ceramic filter passes only the 250 kHz-wide difference-frequency band centered at 10.7 MHz. This second IF is applied to the 10.7/455 converter (A3) where it is mixed in the third double-balanced mixer with an 11.155 MHz fixed-frequency synthesized LO input to produce the final IF of 455 kHz. The low-pass filter after the mixer rejects mixer sum and feed-through products, permitting only the desired signals at or near 455 kHz to pass.

Tuning is accomplished by varying the frequencies of the synthesized LO inputs applied to the first and second double-balanced mixers. The LO input to the first mixer covers the 83.310-113.310 MHz range in discrete 10 kHz increments. For finer resolution, the LO input to the second mixer covers the

72.110-72.100 MHz range (a 10 kHz spread) in 10 Hz increments. As the operator tunes the receiver upward in frequency, the second LO frequency decreases from 72.110 MHz in 10 Hz increments until it reaches 72.100 MHz. At this point, the first LO frequency which was constant, automatically advances by one 10 kHz increment while the second LO frequency resets to 72.110 MHz and continues decreasing in 10 Hz increments as before as the operator continues tuning the receiver upward. If the operator tunes the receiver lower in frequency, the above process is reversed. In this manner the entire 0.5-30.5 MHz tuning range of the receiver is covered in 10 Hz increments without the need for band changing. To eliminate sideband inversions, it is necessary that the synthesized LO frequencies move in opposite directions during receiver tuning.

The output of the low-pass filter on the 10.7/455 converter (A3) is available as a 455 kHz signal monitor output for use with an external panoramic display unit. The 455 kHz signal is also applied to the input of one of six digitally-selectable IF filters. The four filters supplied with the receiver have 3 dB bandwidths of 0.5, 2.0, 4.0, and 8.0 kHz respectively; bandwidths of the remaining two filters (if desired) are determined by the user. After being amplified by the 455 kHz IF amplifier (A8), the IF signal is applied simultaneously to AM, FM, CW/USB and LSB demodulators.

The AM demodulator employs a full-wave diode envelope detector to recover the audio modulation from the carrier. A noise limiter circuit included in the AM demodulator can be activated to reduce impulse-type noise. The FM demodulator employs a symmetrical IC limiter and discriminator circuit. For CW/USB/ LSB demodulation, a 455 kHz variable or fixed BFO signal is combined with the IF signal in a product detector to produce a demodulated audio output. Separate demodulators are used for CW/USB and LSB detection.

All demodulator outputs are applied to a digitally-controlled switch, which routes the selected demodulator output signal to the audio amplifier (A13). The audio amplifier builds up the signal to a level sufficient to drive a pair of headphones and also provides a line audio output. The selected demodulator output from the digitally-controlled switch is also applied to the gain control circuit (A14) which uses this signal to produce the AGC voltage outputs applied to the RF and IF sections. Three gain control modes are available - normal AGC (fast-attack fast-decay), hold AGC (fast-attack delayed-decay), and manual gain control (receiver gain adjustable by the RF GAIN control on front panel). In the ISB detection mode, the receiver gain mode is automatically set to normal AGC while independent fast-attack slow-decay AGC loops in the SSB demodulators are activated. The front panel meter may indicate either the signal strength or audio level.

4.3.2 SCHEMATIC DESCRIPTIONS.

4.3.2.1 Type 791312 0.5-30 MHz Bandpass Filter (A20). - Figure 7-32 is the schematic diagram for the 0.5-30 MHz bandpass filter. Signals from the antenna are applied to the five-pole filter through J1. The filter actually consists of a high-pass filter with a cut-off frequency just below 0.5 MHz in tandem with a low-pass filter with a cut-off frequency just above 30 MHz. The combined

responses of these filters result in the desired 0.5-30 MHz bandpass characteristic. Signals in the 0.5-30 MHz range leave the filter at J2, and are applied to the sub-octave preselector filters on the input filter assembly (A1).

4.3.2.2 Type 791199 Input Filter Assembly (A1). - Figure 7-1 is the schematic diagram for the input filter assembly. Signals from J2 of the 0.5-30 MHz bandpass filter (A30) are applied to J1. The filter assembly mounts a mother board (A1) which in turn mounts four filter boards (A1A1, A1A2, A1A3, and A1A4). The RF input from J1 is applied to all four filter boards simultaneously. Each filter board contains two sub-octave filters. Diode switches at the input and output of each sub-octave filter are digitally controlled by a three bit binary word (2^0 , 2^1 , 2^2) at the control input from the receiver register board. An integrated circuit on the 10-18/18-30 MHz filter board (A1A1) decodes the binary word and causes another integrated circuit on one of the four filter boards to forward bias the diode switches of the correct sub-octave filter, while holding the diode switches of the remaining sub-octave filters reverse biased so that no signals will pass through them. Thus, signals pass through only the correct sub-octave filter.

Type 791247 10-18/18-30 MHz Filter (A1A1A1). - Figure 7-2 is the schematic diagram for the 10-18/18-30 MHz filter. Two elliptical function sub-octave filters are contained on the board, each consisting of three low-pass sections followed by three high-pass sections. The RF signal output from the 0.5-30 MHz bandpass filter (A30) is applied simultaneously to both sub-octave filter inputs (as well as to the six sub-octave filter inputs on the other three boards). Diode switches at each filter input, however, prevent the RF signal from passing to all but the selected sub-octave filter. Assuming that the 18-30 MHz filter has been selected, pin 5 (2Y) of U1 is in the on state (at ground potential) resulting in electron flow from that point through R2 and L5. From L5, electrons flow to the +5 V supply source through two parallel branches. One of these branches comprises series circuit CR2, CR1, and L1. The other comprises series circuit CR5, L4, and R18. The resulting 80 mA of current through each diode results in a heavy forward bias which in turn permits the RF input to pass through diodes CR2 and CR5 to the filter (the heavy forward bias results in the high dynamic range of the diodes). L1, L4, and L5 are RF chokes which isolate the signal path from the dc control path. An identical diode switch at the filter output permits the RF signal to pass through C35 to the output of the filter board. The 10-18 MHz filter, however, is isolated from the RF input by the reverse bias on its switching diodes (CR3, CR4, CR6, CR9, CR10, and CR12). Since pin 3 (1Y) of U1 is in the off state, no current flows in or out of that terminal. As a result, the +15 V supply source reverse biases the diodes through R4, thus isolating the 10-18 MHz filter from the RF signal input and output. The remaining six sub-octave filters on the other filter boards are similarly switched out of the signal path. The diode switches are designed so that the series diodes (CR2, CR3, CR5, CR6, CR7, CR8, CR9, and CR10) perform the actual RF signal switching, while the shunt diodes (CR1, CR4, CR11, and CR12) prevent corresponding RF chokes L1, L2, L24, and L25 from interacting with other filter inputs. For

example if the 10-18 MHz filter is being used, the reverse bias on CR1 in the 18-30 MHz filter prevents RF choke L1 from effectively shunting the input of the 10-18 MHz filter. The Y outputs of one-of-eight decoder U1 are controlled by the corresponding A inputs (see Table 4-1). Since the B inputs are grounded, it is only necessary to ground the A inputs to turn on (ground) the Y outputs. The A inputs in turn are controlled by U2 outputs 0 and 1 (U2 outputs 2-7 perform the same function for the other three filter boards). U2 outputs 0-7 are controlled by a 3 bit binary word at control inputs A, B, and C (see Table 4-1). The digital word determines which one of U2's outputs (0-7) is low (all others are high). The single low output of U2 determines which Y output of U1 is grounded (turned on), and consequently, which sub-octave filter is selected. The control inputs to U8 come from the receiver register.

Type 791250 3.4-6.0/6.0-10 MHz Filter (A1A1A2). - Figure 7-3 is the schematic diagram for this filter board. It is functionally identical to the filter board described above. Some component values are different as a result of the different frequency coverage. Decoding of the digital word from the receiver register is done by A1A1A1U2 as previously described.

Type 791249 1.2-2.0/2.0-3.4 MHz Filter (A1A1A3) and Type 791248 0.5-0.8/0.8-1.2 MHz Filter (A1A1A4). - Figures 7-4 and 7-5 are the respective schematic diagrams for these filter boards. Since these filters are very similar to the ones described above, no further circuit discussion is required.

4.3.2.3 Type 79116 Input Converter (A2). - Figure 7-6 is the schematic diagram for the input converter. The signals from the input filter assembly (A1) are amplified and up-converted to the 82.805 MHz first IF. The 82.805 MHz IF is applied to a 35 kHz bandwidth filter and then amplified. The amplified band-limited IF is then applied to a PIN diode attenuator controlled by the RF AGC voltage (shaped for the desired AGC characteristic by attenuator shaper A1). After another stage of amplification, the 82.805 MHz IF is down-converted to 10.7 MHz. The 10.7 MHz second IF leaves the input converter after passing through a 250 kHz bandwidth ceramic filter.

RF Amplifier. - Incoming signals at J1 are applied to the RF amplifier through a 32 MHz cut-off frequency low-pass filter composed of C10, C11, and L1. The low-pass filter reduces LO-to-antenna conduction and improves RF image rejection. Q2 is a common gate amplifier source-biased by constant current generator Q1. Diode CR1 minimizes Q1 collector current changes due to temperature by changing base bias on Q1 to counteract the normal change with temperature in Q1 collector current (a rise in temperature causes CR1 to develop a lower forward voltage drop, thus lowering the base bias of Q1 in the same proportion as Q1's base-emitter voltage, thereby maintaining a constant voltage across R4). Similarly, a reduction in temperature results in a higher base bias on Q1, thus compensating for the normal decrease with temperature in Q1 collector current. Thus, the operating point of Q1 (and therefore Q2) is stabilized over a wide temperature range. L4 and T1 comprise a broadband impedance matching network

Table 4-1. Truth Tables for Input Filter Logic Elements

SN75453P (U1)

A	B	Y
0	0	0 (ON)
0	1	1 (OFF)
1	0	1 (OFF)
1	1	1 (OFF)

NOTE: "0" Indicates Ground Potential
"1" Indicates A Positive Potential

8250 (U2)

INPUTS			OUTPUTS*								FILTER FREQUENCY MHz
$A(2^0)$	$B(2^1)$	$C(2^2)$	0	1	2	3	4	5	6	7	
0	0	0	0	1	1	1	1	1	1	1	18-30
1	0	0	1	0	1	1	1	1	1	1	10-18
0	1	0	1	1	0	1	1	1	1	1	6.0-10
1	1	0	1	1	1	0	1	1	1	1	3.4-6.0
0	0	1	1	1	1	1	0	1	1	1	2.0-3.4
1	0	1	1	1	1	1	1	0	1	1	1.2-2.0
0	1	1	1	1	1	1	1	1	0	1	0.8-1.2
1	1	1	1	1	1	1	1	1	1	0	0.5-0.8

*Designations for outputs do not correspond with IC pin numbers.

that is used to couple the output of Q2 to the lower impedance input of mixer U1. R1 functions as a parasitic suppressor, while R5 loads L2 to prevent resonant effects. R6 establishes the output impedance of Q2.

First Mixer, LO Amplifier. - Double-balanced mixer U1 combines the RF amplifier output with the 83.310-113.310 MHz LO input from LO amplifier A3Q2 to produce the 82.805 MHz first IF. 35 kHz bandwidth filter FL1 passes the difference frequencies while attenuating sum and other mixer products. L9-C23 and L10-C24 tune the filter input and output, respectively. The LO amplifier increases the amplitude of the 83.310-113.310 MHz synthesized LO input to the 27-30 dBm level required by double-balanced mixer U1. A3Q2 operates as a common emitter stage base-biased by A3Q1. A3CR1 stabilizes the base bias current into A3Q1 against temperature variations in much the same manner as CR1 stabilizes the operating points of Q1 and RF amplifier Q2 as described above. A3R4 and A3L1 introduce degenerative feedback that decreases with frequency resulting in a more uniform output level from A3Q2 over the 83.310-113.310 MHz frequency range. R20, R23, and C28 establish the input impedance of the stage.

82.805 MHz IF Amplifiers, PIN Diode Attenuator. - The output of FL1 is applied to common gate 82.805 MHz IF amplifier Q5. CR2 and Q4 provide temperature-stabilized source bias for Q5 in the same manner as CR1 and Q1 provide temperature-stabilized source bias for RF amplifier Q2. The drain circuit consists of a parallel resonant tank provided by the shunt combination of C30 and C31 effectively in parallel with T2 (one end of T2 is grounded by C29). A tap on T2 matches the high impedance output of Q5 to the low impedance present at the PIN diode attenuator input. The attenuator is composed of three PIN diodes arranged in a pi configuration. The PIN diodes act as voltage-controlled variable resistors. The control voltage is derived from the AGC input to the attenuator shaper stage, which shapes the AGC input for a more suitable RF AGC characteristic. Attenuation is increased by increasing forward bias on the shunt diodes (CR3 and CR5) and reducing forward bias on the series diode (CR6). The attenuator shaper will be discussed in a separate paragraph. The attenuator output is applied to IF amplifier stage Q7 which is identical in operation to IF amplifier Q5 described above. The low impedance output from T3 is applied through C40 to second mixer U2.

Second LO Amplifier, Second Mixer. - The 72.110-72.100 MHz second LO input from the synthesizer is applied to the base of Q3. R21 establishes the correct termination impedance for the synthesizer. Q3 is a common-emitter amplifier stage with degenerative feedback introduced in the emitter circuit by R25 for gain stabilization. The output is developed across a resonant tank circuit composed of C53 and L6. C54 couples the output of the stage to a 15 kHz bandwidth 72.105 MHz center frequency filter. R27 provides the correct input termination for the filter. L7 and C56 tune the filter output which is coupled through C55 and FB5 (a ferrite bead) to the base of Q8. Q8 operates in a manner very similar to Q3. R32 provides degenerative feedback for amplifier gain stabilization. The output is developed across a tank circuit comprising C60, C61, C62,

and L24. C58 is a neutralization capacitor. C61 and C62 form a capacitive voltage divider that matches the output impedance of Q8 to the lower input impedance of Q9. Q9 is a common base amplifier stage. Base bias is developed through R35, R38, and CR4 (a temperature stabilizing diode). C65 holds the base at RF ground. Emitter resistor R34 is a parasitic suppressor. The collector output of Q9 is impedance matched to the LO input of the second mixer by means of the pi network comprising C66, C69, and L26. R40 provides a resistive termination for the network input. The second LO signal is mixed with the 82.805 MHz IF in double-balanced mixer U2. The mixer outut is applied to 250 kHz bandwidth 10.7 MHz filter A2FL1. The pi networks at the input and output of the filter match the high impedance filter to the 50 ohm output circuit of the second mixer. The 10.7 MHz second IF signal is then passed to the 10.7/ 455 converter (A3)

Attenuator Shaper (A2A1). - Figure 7-7 is the schematic diagram of the attenuator shaper. For the purposes of this circuit description, the schematic has been redrawn as shown in Figure 4-3. R22 drops the -15 V dc supply input to -6.3 V dc (stabilized by zener diode VR1). The voltage divider composed of R20 and R21 results in a -1.5 V dc bias on the anode of CR3. AGC voltage, varying from a no-signal level of 0 volts to a strong-signal level of -10 volts is applied at E5 to the input circuitry of amplifier U1B. Since U1B is a linear inverting amplifier, the output voltage should be in linear inverse proportion to the AGC voltage input. This linear relationship exists until the AGC input voltage at E5 causes the voltage at the cathode of CR3 to become more negative than the -1.5 V dc bias on the anode. When this happens, CR3 becomes forward biased causing an increased voltage drop across R15 and R16, thus increasing AGC input voltage attenuation and reducing the net amplifier gain. As a consequence, the output voltage of U1B at E2 rises in linear inverse proportion to the applied AGC input until CR3 becomes forward biased, resulting in a +6.8 V dc "break point" at U1's output. A further increase in AGC voltage results in greater output from U1B, although the output increases at a lower rate due to the lower amplifier gain caused by CR1 after the "break point" voltage is reached. This shaped voltage is applied to the inverting input of U1A through R13 and R4. Under 0 V dc AGC input conditions, the output of U1A is at its quiescent level of +5.8 V dc due to the negative bias applied to the inverting input through R5. The negative bias is taken from the voltage divider comprising temperature-stabilizing thermistor RT1 and R10. The +5.8 V dc output of U1A results in cathode biases of +3.35 V dc and +5.0 V dc on CR1 and CR2 respectively, while both anodes are biased at a level just under 0 V dc (the quiescent output level of U1B). As the AGC voltage at E5 becomes negative, the anode voltage of CR1 and CR2 rises. At the same time, the inverted output of U1A causes the cathode voltages of CR1 and CR2 to fall. Eventually, CR1 becomes forward biased, effectively shunting R7 across R2, increasing amplifier negative feedback and reducing gain, (i.e., establishing a "break point" in the amplifier output characteristic). As the AGC voltage at E5 continues to become more negative, CR2 will also become forward biased, establishing another "break point". The E2 output (with a single "break point") is applied to the shunt diodes in the PIN diode attenuator. The E1 output is a composite of the characteristics of U1A and U1B, and exhibits three break

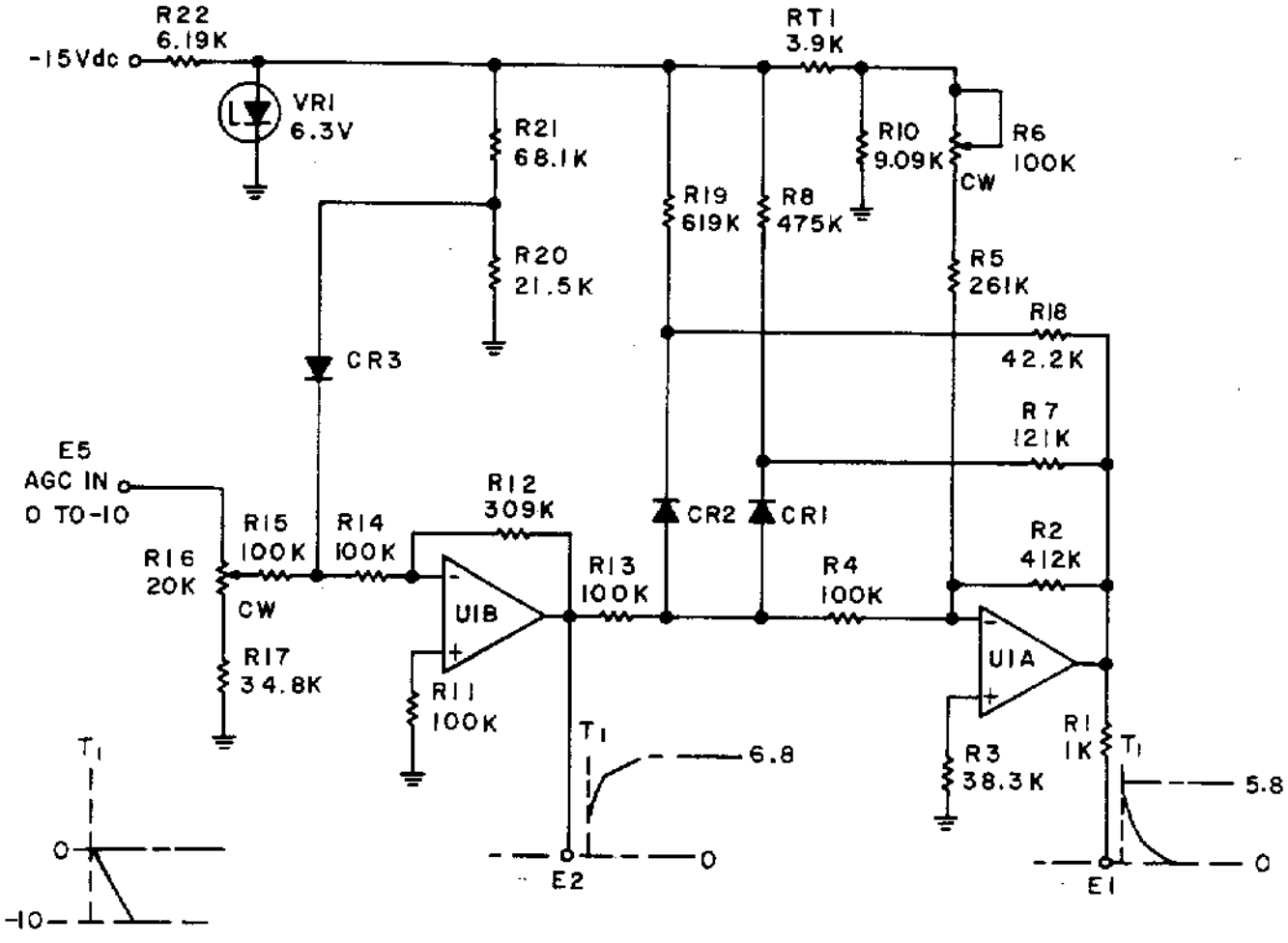


Figure 4-3. Simplified Schematic Diagram of Attenuator Shaper

points and four slopes. This output is used to control the series diode in the PIN diode attenuator. The shunt diode is controlled by the output of U1B.

4.3.2.4 Type 791198 10.7/455 Converter (A3). - Figure 7-8 is the schematic diagram for the 10.7/455 converter. The 10.7 MHz IF from J2 of the input converter (A2) is amplified, filtered and down-converted to 455 kHz. The 455 kHz third IF is filtered and amplified before being passed to the next receiver stage.

Q1 and Q2 comprise a 10.7 MHz cascode amplifier. The 10.7 MHz second IF is applied to the base of Q1 through C1. R2 and R3 form a base-bias voltage divider for Q1. R1 and C2 form a degenerative feedback path that improves the signal handling capability of the stage. Degenerative feedback in this form, however, lowers the input impedance of the stage. To counteract this, unbypassed emitter resistor R4 is used to introduce degenerative feedback which raises the impedance of the stage. The output of the cascode stage is developed across RF choke L2 and applied to an impedance-matching pi-network comprising C7, C8, and L3. R7 establishes the output impedance of Q2. FL1 is a 250 kHz

bandwidth ceramic filter. C9, C10 and L4 match the output impedance of the filter to the lower input impedance of mixer U1.

The 11.155 MHz LO input from the synthesizer is applied to the base of Q5 through C29, Y1, and C20. Y1 serves as a series resonant filter to suppress spurious inputs from the synthesizer. R29 and R13 establish the termination impedances for the filter, while C29 is used to tune the filter to precisely 11.155 MHz. Q5 is a common-emitter amplifier stage. R18 developes negative feedback. Collector output is developed across L10, which resonates with circuit capacitances to 11.155 MHz. The output of Q5 is applied through R19 and C23 to the base of Q6. Q6 is a common emitter amplifier stage similar to Q5. Collector output is applied to the LO input of balanced mixer U1 through an impedance matching network comprised of C27, C28, and L12, and a 3 dB pad comprising R26, R27, and R28. R23 is a parasitic suppressor.

U1 mixes the 10.7 MHz IF with the 11.155 MHz LO input to produce sum and difference frequencies. A low-pass filter and impedance matching network comprising C12, C13, C14, L5, and L6 attenuates the sum component while permitting the 455 kHz difference component to pass to the input of common gate amplifier Q4. Temperature-stabilized source bias for Q4 is provided by constant current generator Q3 and temperature compensating diode CR1.

4.3.2.5 Type 72399-(X) IF Filter Assembly (A4, A6). - Figure 7-9 is the schematic diagram for the IF filter assembly. The assembly consists of two identical boards (A4 and A6), each mounting up to three 455 kHz mechanical filters. Control voltages from the receiver register are used to switch the selected filter into the signal path. Relays at the input of each filter are used for input switching while FET amplifiers are used for output isolation. Filter control outputs are applied to a subsequent IF amplifier stage, and activate either a narrowband or wideband IF amplifier, depending upon the bandwidth of the selected IF filter. This will be discussed in more detail under the 455 kHz IF amplifier (A8) circuit description.

The 455 kHz IF signal from the 10.7/455 converter (A3) is applied simultaneously to relays K1, K2, and K3. Detail A on the schematic diagram shows the internal wiring of the normally open, SPST relays. Assuming that IF filter FL1 has been selected, a voltage from the receiver register is applied to the base of Q1 (the bases of Q4 and Q7 remain at ground potential), turning this transistor on. Most of Q1's collector current flows through the base-emitter junction of Q2, causing it to saturate. Since the coil of relay K1 is in the collector circuit of Q2, K1 is activated, permitting the 455 kHz IF signal to be applied to FL1, and to gate #1 of isolation amplifier Q3. The positive voltage drop across the series combination of R5 and the relay coil is applied through R8, R11, and R12 to gate #2 of Q3, turning this amplifier on and permitting the IF signal at gate #1 to be amplified and applied to the next stage through R48 and C24. Since Q6 and Q9 receive 0 volts bias on gate #2 and the sources are all positively biased by R30, very little drain current flows, minimizing interaction with Q3. CR1 protects Q2 from potentially large negative voltages induced by the collapse of the magnetic field of K1 when the relay is de-energized. CR2 is part of an AND gate circuit. R12 is an IF gain adjustment. Operation of the other filter/

amplifiers is the same as described above. R12, R28, and R43 are IF gain adjustments set to equalize the gain of the filter amplifiers.

4.3.2.6 Type 72409 455 kHz IF Amplifier (A8). - Figure 7-11 is the schematic diagram for the 455 kHz IF amplifier. The first two stages are gain controlled dual-gate MOSFET amplifiers. The output of Q2 is applied simultaneously to a narrowband IF amplifier comprising Q3 and Q5, and a wideband IF amplifier comprising Q4 and Q6. The amplifier used is determined by the filter control outputs from A8. These switched outputs are wired to provide base bias for either the wideband or narrowband amplifiers, activating one and disabling the other. The wideband amplifier is activated when the filters greater than 2 kHz bandwidth are used, while the narrowband amplifier is activated when the 2 kHz or narrower bandwidth filters are used.

Q1 and Q2 are cascaded gain-controlled MOSFET amplifiers. The 455 kHz signal from the IF filter assembly is applied through C1 to gate #1 of amplifier Q1. The drain output of Q1 is developed across L1 and applied through C6 to gate #1 of Q2. The drain output of Q2 is developed across L2. IF output is taken from the arm of gain control potentiometer R16. Gate #1 bias for Q1 and Q2 is developed by voltage dividers R1-R2 and R9-R10 respectively. Gate #2 of Q1 is biased at approximately +3.5 V dc by R3, R5, and CR1 at 0 V AGC input. The bias on gate #2 of Q1 does not fall until the AGC voltage becomes sufficiently negative to reverse bias CR1, effectively removing it from the circuit. Further negative increases in AGC voltage will then be reflected in a more negative bias on gate #2 of Q1, reducing the amplifier gain. Identical AGC circuitry is used for Q2.

The IF signal output from Q2 is applied simultaneously to narrowband and wideband IF amplifiers comprising Q3-Q5 and Q4-Q6, respectively. As mentioned above, switched +15 V dc supply lines determine which of the two amplifiers will be activated (activation is achieved by applying the switched +15 V dc source to the base bias voltage divider of the desired amplifier). Assuming that the wideband amplifier (Q4-Q6) is activated, the IF signal is amplified by common emitter amplifier Q4. R32 provides degenerative feedback for improved signal handling capability, while R34 and R28 act as parasitic suppressors. Tank circuit C22-L5 develops the collector output. C25 couples the signal to an impedance matching network composed of L6, C26, and C27, which steps down the circuit impedance. Loading resistor R36 broadens the frequency response of the interstage coupling network. Output is provided by emitter follower amplifier Q6. Operation of the narrowband amplifier (Q3-Q5) is very similar to that of the wideband amplifier, although some component values differ, and no loading resistor is used. Interaction between the amplifier outputs is minimized due to the isolation provided by the reverse bias on the base-emitter junction of the inactive emitter follower.

4.3.2.7 Type 791113 AM Demodulator (A9). - Figure 7-12 is the schematic diagram of the AM demodulator. The 455 kHz IF signal is amplified and applied to a diode detector. The resultant audio signal is then amplified. A noise limiter in the audio section reduces the intensity of impulse-type noise.

The 455 kHz signal from the 455 kHz IF amplifier (A8) is applied to gate #1 of Q1 through C1. Q1 is a common source amplifier, with its drain output developed across L1. R9 loads L1 to reduce resonant effects. Bias for gate #1 of Q1 is obtained from voltage divider R1-R2. Gate #2 is used for gain control. The output of Q1 is applied to the base of isolation amplifier Q2.

Q2 develops both emitter and collector outputs, each 180° out of phase with the other. The emitter output drives Q4, another isolation amplifier. The emitter output of Q4 is coupled through C16 to board pin 5 (IF OUTPUT), and then routed to the LSB, USB/CW, and FM demodulators. The collector output is transformer coupled, and made available as an IF output at board pin 1. From board pin 1, the IF signal is routed to the IF OUTPUT jack (J8) on the main chassis.

The collector output of Q2 is applied through C7 to the base of common emitter amplifier Q3. Base bias is developed by R15-R16. R22 introduces degenerative feedback. The collector output is developed across the primary of T1 and its resonating capacitor, C24. R21 is a parasitic suppressor. R36 loads the resonant output circuit to optimise the frequency response.

The AM detector is a full-wave center-tapped rectifier circuit. Diodes CR3 and CR4 are used as detectors (rectifiers). A slightly positive bias is applied to the anodes of the diodes to overcome the diode barrier potentials to increase linearity and measure the sensitivity of the detector. The rectified output is developed across R27. C14 filters out the 455 kHz component of the rectified output. This rectified and filtered signal is then applied to emitter follower Q5.

The AM detector output from Q5 is applied to a noise limiter circuit comprising CR5, CR6, Q6, Q7, Q8, and associated resistors and capacitors. When activated, the noise limiter limits man-made and atmospheric impulse-type noise to just under twice the average AM detector output level (approximately 90% of the peak AM detector output level).

For clarity, a simplified noise limiter circuit diagram is presented. Referring to Figure 4-4, assume that the noise limiter has been activated (this will be explained in the following paragraph). The (positive) AM detector output of Q5 is applied to time constant circuit R31-C17. The long time constant results in C17 being charged to the average AM detector output voltage. The AM detector output of Q5 is simultaneously applied to voltage divider R32-R33. The ratio of R32 and R33 is such that for a 90% modulated AM signal, the resultant peak voltage at the cathode of CR5 is approximately equal to the average voltage at the anode of CR5. Consequently, CR5 will be forward biased as long as the AM detector voltage at the cathode of CR5 is not greater than the 90% modulation level. Disregarding for the moment the 0.6 V diode barrior potential that must be overcomve, the forward biased diode will permit the detected AM voltage to be passed through CR5 and R26 to audio amplifier U1. If a sudden noise pulse occurs, the signal voltage at the cathode of CR5 rises accordingly. The long time constant of R31 and C17, however, prevents the average voltage through R48 at the anode of CR5 from also rising. Since the diode becomes momentarily reverse biased, no output is applied through R26 to audio amplifier U1. Thus, sudden noise burst are limited in amplitude to 90% of the peak demodulated signal voltage, resulting in effective noise limiting.

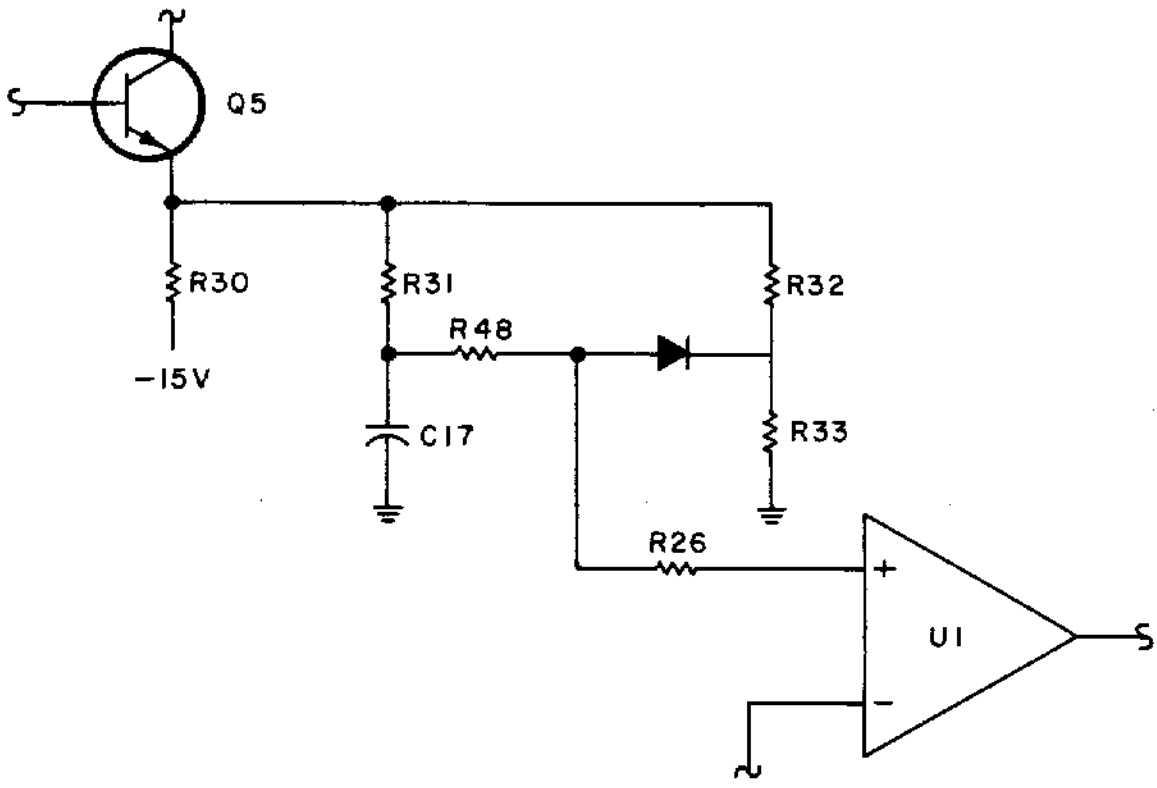


Figure 4-4. Noise Limiter, Simplified Diagram

The simplified circuit is modified somewhat to provide a means of eliminating the effect of the barrier potential of CR5 and switching the noise limiter on or off as desired. Referring back to Figure 7-12, the positive AM demodulator output of Q5 is applied to averaging circuit R31-C17, just as in the simplified circuit. The averaged output voltage from C17, however, is applied through R48 to the anode of CR5 via emitter follower Q7. Q5's output voltage is also applied to the cathode of CR5 via R32 and R33, with C22 providing high frequency roll-off. In the simplified circuit diagram the voltage dividing action of R32 and R33 reduced the signal voltage at the cathode of CR5 to the point where an AM detector output signal of 90% modulation or less resulted in a lower voltage on the cathode of CR5 than on the anode. In order for the diode to conduct, however, a forward bias of 0.6 volts is required to overcome the diode barrier potential. Thus in the simplified circuit diagram, the barrier potential would require a lower voltage at the cathode of CR5 for conducting to begin. This directly implies then that the signal level at which CR5 would reverse bias would be lower, thus resulting in limiting occurring at signal modulation levels well under 90%. This would be undesirable since the clipped signal would be distorted. In the actual circuit, the diode barrier potential is counteracted by the 0.6 volt base-emitter drop of Q7, which raises the anode voltage of CR5 by 0.6 volt, thus negating the effect of the barrier potential of CR5.

The noise limiter is activated by a positive input (from the receiver register) to board pin 4 (AM NL) that turns Q6 on and Q8 off. Under these circumstances, the noise limiter operates as described above. To disable the noise limiter, a ground potential (from the receiver register) is applied to board pin 4 (AM NL) that turns Q6 off and Q8 on. This results in a positive voltage applied to the base of Q7 through Q8, CR6, and R49. The increased positive voltage at the base of emitter follower Q7 causes the emitter voltage of that transistor to rise by a like amount, resulting in a positive bias applied to the anode of CR5 through R48. The magnitude of this positive bias is sufficient to forward bias CR5 under all signal conditions, effectively disabling the noise limiter.

U1 is an audio amplifier with a high impedance input and a low impedance output. The AM DET OUTPUT (board pin 8) is applied to the gain control board (A14) while the AM DET MONITOR (board pin 12) output is routed to the AM MONITOR jack (J7) on the receiver main chassis. R39-C20 and R40-C21 are low-pass filters used to provide high frequency roll-off.

4.3.2.8 Type 791162 FM Demodulator (A10). - Figure 7-13 is the schematic diagram of the FM demodulator. The input comes from the IF output amplifier on the AM demodulator board (A9). The 455 kHz IF signal is limited in amplitude by a high gain limiting amplifier and demodulated in an FM detector. The resultant audio is then amplified.

The 455 kHz IF signal from the AM demodulator is applied through C1, R1 and C2 to the input of U1. U1 functions as a high gain symmetrical current mode limiter. The limiting action results in a constant output amplitude over a wide range of input signal amplitudes, thus ensuring that all AM signal components are eliminated.

After limiting, the signal is passed to the Foster-Seely FM discriminator. Discriminator transformer T1 has both its primary and secondary circuits resonated at 10.7 MHz. C10 introduces a quadrature component of the primary voltage to the secondary center tap. This causes the primary voltage of T1 to be 90° out of phase with the entire secondary voltage at the 455 kHz center frequency. The vectoral addition of these voltages results in equal amplitude ac voltages at the anodes of CR1 and CR2. The resultant rectified dc voltages are of equal amplitude and opposite polarity, and therefore cancel, resulting in no output to U2. If the signal frequency deviates from the 455 kHz center frequency, the 90° phase relationship changes, with the result that the voltage amplitude at the anode of one of the diodes will exceed that of the other. As a consequence, the rectified dc voltages will reflect the amplitude difference, and a net output to U2 will result. Since the instantaneous output voltage is proportional to the frequency difference between the instantaneous signal frequency and the 455 kHz center frequency, the resultant output in effect is a reproduction of the modulation of the FM carrier. C13 helps to filter out 455 kHz signal components.

The demodulated signal is passed to voltage follower U2. The two available audio outputs are the FM DETECTOR MONITOR output (routed to J9 on the main chassis) and the FM AUDIO output, which is applied to the audio amplifier (A13).

Q1, Q2, Q3, and Q4 comprise a switched 455 kHz IF amplifier that is active only during either CW mode. It's purpose is to provide an IF signal to the USB/CW demodulator that bypasses the 2.7 kHz bandwidth USB filter (see Figure 7-14), since this filter would otherwise cause gain variations across the IF passband in CW operation. A positive output level (generated in the CW modes only) at board pin 7 (CW(s)) activates a diode switch in the USB/CW demodulator that shunts the USB filter, eliminating any 455 kHz feedthrough from that source.

Referring back to Figure 7-13, the 455 kHz IF input to the FM demodulator is also applied through R17 and C16 to the base of Q3, a common emitter amplifier with degenerative feedback introduced into the emitter circuit by R23. The collector output of Q3 is dc coupled to the base of emitter follower Q4. The output of Q4 is applied through C20 and R26 to the CW input of the CW/USB demodulator. Q3 and Q4, however, can only amplify the 455 kHz signal if the receiver is in either CW mode of operation. Assuming that a CW mode has been selected by the operator, either the CW V (CW mode using the variable frequency BFO) or the CW F (CW mode using the fixed frequency BFO) inputs at board pins 15 and 16 respectively will be positive. The positive input causes collector current to flow through Q1, which also turns on Q2. As long as Q2 remains on, Q3 and Q4 will receive the positive voltage required for operation, and will function as described above. The switched voltage is also applied through CR6 to board pin 7, and routed to the CW/USB board. If the CW V and CW F inputs are disabled (grounded), however, Q1 and Q2 will no longer conduct, resulting in amplifiers Q3 and Q4 being disabled and no positive output at board pin 7. The CW V and CW F inputs are controlled from the receiver register.

4.3.2.9 Type 791180-(X) LSB/USB/CW Demodulator (A11, A12). - Figure 7-14 is the schematic diagram of the LSB and USB/CW demodulators. Other than the difference in component values shown on the schematic, both demodulators are identical. For either LSB or USB reception, the 455 kHz IF signal from the AM demodulator (A9) is amplified and applied to 2.7 kHz bandwidth filter (the center frequency of the LSB filter differs slightly from that of the USB filter) and then to a double-balanced modulator/demodulator where the signal is mixed with the BFO input. The audio (difference) frequency output of the double-balanced modulator/demodulator is then amplified and made available as two audio outputs. The audio signal is also applied to an AGC detector and amplifier, and the resulting AGC voltage is used to control the gain of the input 455 kHz amplifier stage if the ISB detection mode has been selected. The USB demodulator is also used for demodulation of CW signals, as will be explained in detail in a subsequent paragraph.

The 455 kHz IF signal from the AM demodulator (A8) is applied to voltage divider R1-R2. The attenuated signal is then applied through C1 to gate #1 of Q1. Voltage divider R3-R4 provides the proper dc bias for gate #1. The amplified signal is developed across L1 and R5, and coupled through C5 to the base of Q2. L1 resonates with internal and circuit capacitances to 455 kHz, while R5 loads L1 to broaden the bandpass. Q2 is a common emitter amplifier stage with degenerative feedback introduced into the emitter circuit by R13 and R14. R14 controls the stage gain by varying the amount of degenerative feed-

back. Collector output is developed across R11 and applied to bandpass filter FL1 through C9. Voltage divider R8-R9 provides base bias for Q2.

The bandpass of FL1 on the LSB board (A12) extends approximately from 452.0-454.7 kHz, while the bandpass of FL1 on the USB/CW board (A11), extends approximately from 455.3-458.0 kHz. C10 and C12 are filter termination capacitors. The filter output is coupled through C27, C28, R22, and C15 to the input of double-balanced modulator/demodulator U1. For LSB or USB reception, CR5 is reverse biased by the negative voltage at its anode produced by current flowing through R65 and R66 to the (grounded) CW(S) terminal (board pin 19). The CW(S) input comes from the FM demodulator board, and is held near ground potential in the LSB and USB modes of operation. As a result, CR5 has no effect on circuit operation for these modes of reception. For CW reception, however, a positive voltage at the CW(S) input (from the FM demodulator board) forward biases CR5, causing the output of FL1 to be shunted to ground, preventing any FL1 output from reaching U1. Instead, the 455 kHz IF signal from the switched IF amplifier on the FM demodulator board (A10) applied to the CW IF INPUT (board pin 5) is applied through C25 and C15 to the signal input of U1.

U1 receives the IF signal at pin 1 and mixes it with the BFO signal applied to pin 7. The BFO signal (from the BFO synthesizer) is first amplified by common emitter stage Q3. R17 and R18 form a base bias voltage divider, R21 develops degenerative feedback for the stage, and R20 is the collector load resistor. The collector output is applied through C14 to pin 7 of U1. The output of U1 at pin 9 contains sum and difference frequencies, but C19 prevents the sum frequency from being passed. Only the audio difference frequency is coupled through C20 and R33 to the input of audio amplifier U2. VR1 drops the -15 V dc supply to approximately 8.2 volts, and applies this voltage to pin 10 of U1. R24-R25 and R26-R27 are voltage dividers that are used to provide proper biasing voltages for U1, R28 establishes the conversion gain, and R30 and R31 are the load resistors for the differential output. Since only a single-ended output is required, C17 is used to RF bypass pin 6 of U1. R31 is a voltage dropping resistor, R29 establishes the internal bias of U1, and L2 is an RF choke that holds the BFO input of U1 (pin 7) at dc ground potential.

Audio amplifier U2 uses a frequency sensitive degenerative feedback circuit to produce high frequency audio roll-off. R35, the amplifier negative feedback resistor, is shunted by C21. At low audio frequencies, the reactance of C21 is high compared to the resistance of R35, and can be disregarded. At higher audio frequencies, however, the reactance of C21 becomes sufficiently low to significantly increase the inverse feedback (and reduce the gain) of U2. Thus, high audio frequencies receive less gain. The audio signal is then passed through R37 to the SSB/CW AUDIO output terminal (board pin 6). The audio signal is also applied through R38 to T1. The SSB/ISB OUTPUT from the secondary of T1 is made available as an audio output at J10 of the main chassis (AUDIO OUTPUT).

An AGC circuit is comprised of Q4-8, CR1-4, U3 and associated components. The audio output of U2 is detected, processed, and applied to gate 2 of Q1 to provide independent AGC action for the demodulator in the ISB mode of operation.

The output of U2 is applied to the base of Q8. The low impedance emitter output rapidly charges C24 to the peak audio signal level. Since CR6 prevents C24 from discharging into the emitter of Q8 when it becomes less positive than the voltage across C24, the discharge time constant is determined primarily by C24 and R59 (the high impedance input of JFET Q7 can be disregarded). Thus, the AGC detector circuit exhibits the desired fast attack, slow decay characteristic.

High impedance source follower Q7 is employed to provide isolation for the AGC time constant circuit (R59 and C24). The output of Q7 is applied through R56 to the input of emitter-driven amplifier Q6. R39 adjusts the threshold level of the AGC voltage. The collector output of Q6 is developed across R53. This voltage is then applied through R52 to the inverting input of amplifier U3. R51 and R63 cause the output of U3 to be positive under zero-signal input conditions (to properly bias gate #2 of gain-controlled amplifier Q1for ISB operation).

In the ISB mode of operation independent AGC is provided for each sideband demodulator. A switch (activated by the receiver register) raises the gain of Q1 as required to maintain constant output. Thus, the separate ISB AGC loops in the sideband demodulators permit independent AGC action for each received sideband. The remainder of this sub-section discusses the ISB AGC circuitry in greater detail.

If the receiver is operated in any mode other than ISB, the ISB control input (board pin 7) from the receiver register is held near ground potential, shutting off Q4 and Q5. Under these circumstances, current from the -15 V dc supply through R62 flows through CR1, causing a reduction of the positive bias on gate #2 of Q1, reducing Q1's gain and preventing ISB AGC action. In the ISB mode of operation, however, the ISB control input receives a positive voltage from the receiver register turning on Q4 and Q5. This results in a relatively high positive voltage at the collector of Q5 that is applied to the cathode of CR1. Since this voltage exceeds the voltage at the anode, CR1 becomes reverse biased permitting the voltage applied to gate #2 of Q1 to rise to its normal (positive) value as determined by the output of U3. The positive voltage at the cathode of CR2 exceeds the +1.2 volts at the anode (caused by the voltage drop across CR3 and CR4), and CR2 also becomes reverse biased. Thus, the positive gain control voltage applied to gate #2 of Q1 can drop to as low as +0.6 volts (the bias voltage at the anode of CR2 less CR2's 0.6 volt barrier potential) before CR2 becomes forward biased and clamps the voltage at that level. Diode CR2 becomes forward biased when the gain control voltage exceeds approximately +7.0 volts, clamping the voltage at that level.

4.3.2.10 Type 7453 Audio Amplifier (A13). - Figure 7-15 is the schematic diagram of the audio amplifier. The three audio inputs (from the demodulators or gain control board) are applied to a transistor switching network. The selected audio signal is then applied to a squelch gate, after which it is amplified. The amplified signal is made available as the audio line output. Part of the signal is sampled, rectified, and used to drive the audio output meter. Also included on this board is a separate amplifier that is used to build up the level of the audio signal applied to the headphone output circuitry.

The audio inputs to the audio amplifier board come in at board pins 6 (FM), 8 ($\overline{\text{FM}}$ and $\overline{\text{ISB}}$), and 12 (ISB). The FM input comes directly from the FM demodulator (A10). The $\overline{\text{FM}}$ and $\overline{\text{ISB}}$ input comes from the gain control board (A14), where an electronic switch selects either the output of the AM demodulator (A9), or the LSB or USB/CW output from the LSB/USB/CW demodulators (A11, A12) when the LSB, USB, or CCW (but not ISB) mode of operation has been selected.

The audio inputs are applied to an electronic switching network composed of Q1-Q6. The FM audio input is applied through R10 and C1 to the collector of Q5. From this point, it is passed through C4 and R16 to the source of squelch gate Q7. The FM and ISB audio input is applied through R12 and C2 to the collector of Q4. From this point, it is passed through C5 and R17 to the source of squelch gate Q7. Similarly the ISB audio input is applied through R14 and C3 to the collector of Q6. From this point it is passed through C6 and R18 to the source of squelch gate Q7. It is assumed in each case above that Q5, Q4, and Q6 are in the off states. In actual operation, the transistor associated with the selected audio input is off, permitting the signal to be applied to the squelch gate while the other transistors are turned on to short their respective signals to ground. As a result, only the selected signal is passed to the squelch gate.

If the FM detection mode has been selected, a positive potential from the receiver register at board pin 5 (FM) turns Q1 on and Q5 off. With Q5 off, the FM audio input at board pin 6 is free to pass through R10, C1, C4, and R16 to the source of Q7. The near-ground potential at the collector of Q1 places a forward bias on CR1, which lowers the base bias on Q3 (CR1 effectively shunts R8 and R9 when forward biased). As a result, Q3 turns off, permitting a higher potential to be felt at the base of Q4, turning that transistor on. With Q4 on, the $\overline{\text{FM}}$ and $\overline{\text{ISB}}$ audio input at board pin 8 is shunted to ground through R12 and C2. At the same time, board pin 9 (ISB) receives a near-ground potential from the receiver register, holding Q2 in the off state, with the result that Q6 is turned on, shunting the ISB audio input at board pin 8 to ground through R14 and C3. With Q5 off, Q4 on, and Q6 on, the desired FM audio input passes to the source of Q7, while the remaining audio inputs are shunted to ground.

If the ISB detection mode has been selected, a positive potential from the receiver register at board pin 9 (ISB) turns Q2 on and Q6 off. With Q6 off, the ISB audio input at board pin 12 is free to pass through R14, C3, C6, and R18 to the source of Q7. The near-ground potential at the collector of Q2 places a forward bias on CR2, which lowers the base bias on Q3 (CR2 effectively shunts R8 and R9 when forward biased). As a result, Q3 turns off, permitting a higher potential to be felt at the base of Q4, turning that transistor on. With Q4 on, the $\overline{\text{FM}}$ and $\overline{\text{ISB}}$ audio input at board pin 8 is shunted to ground through R12 and C2. At the same time, board pin 5 (FM) receives a near-ground potential from the receiver register, holding Q1 in the off state, with the result that Q5 is turned on, shunting the FM audio input at board pin 6 to ground through R10 and C1. With Q5 on, Q4 on, and Q6 off, only the desired ISB audio input passes to the source of Q7, while the remaining audio inputs are shunted to ground.

If the AM, LSB, USB, or CW detection modes are selected, near-ground potentials from the receiver register are applied to board pins 5 and 9, turning

Q1 and Q2 off. The resulting high potentials at the collector of these transistors cause both CR1 and CR2 to become reverse biased. In turn, full base bias is then permitted to be felt at the base of Q3, turning that transistor on. The resulting low potential at the collector of Q3 turns Q4 off, with the result that the $\overline{FM}$ and $\overline{ISB}$ audio input at board pin 8 is free to pass through R12, C2, C5, and R17 to the source of Q7. At the same time, the high potentials at the collectors of Q1 and Q2 cause both Q5 and Q6 to be turned on, resulting in both the FM and ISB audio inputs at board pins 6 and 12, respectively, being shunted to ground. With Q5 on, Q4 off, and Q6 on, only the desired $\overline{FM}$ and $\overline{ISB}$ audio input passes to the source of Q7, while the remaining audio inputs are shunted to ground.

FET Q7 is the squelch gate that receives the selected audio signal from the audio switching network. With no voltage applied to the gate of Q7 the FET conducts, permitting the selected audio signal to be applied to audio amplifier U2. A negative voltage at the gate of Q7 cuts that transistor off, preventing any audio signals from reaching U2.

U1 is an operational amplifier that is used to control squelch gate Q7. Positive feedback through resistors R21 and R22 set the gain of U1 with a controlled hysteresis. As a result, U1 behaves more as a hysterisis switch than as an amplifier, since a positive voltage at pin 2 (the non-inverting input) causes the output voltage at pin 6 to swing to nearly -15 volts (cutting off Q7), while a negative voltage at pin 2 causes the voltage output at pin 6 to swing to nearly +15 volts. Since CR3 becomes reverse biased, the +15 volt output is not felt at the gate of Q7. The removal of the negative bias from the gate of Q7, however, is sufficient to allow Q7 to conduct. The hystersis caused by the positive feedback applied to U1 prevents the switching threshold from being too narrow.

The input to U2 (pin 2) comes from a voltage divider composed of R19 and R20. R19 receives voltage from squelch control potentiometer on the main chassis (Figure 7-33). The squelch control voltage can be set to any value between 0 and +5 volts. R20 receives gain control voltage from the gain control board (A14). The AGC voltage is negative, and proportional to the average amplitude of the received signal. If the AGC voltage is small, the positive squelch control voltage causes the resultant voltage at the junction of voltage divider resistors R19 and R20 to be positive. As explained previously, a positive voltage applied to inverting input pin 2 of U1 causes the output voltage at pin 6 to become negative, shutting off the squelch gate (Q7) and preventing any audio from reaching the input of the audio amplifier. If the receiver is then tuned to a signal strong enough to produce sufficient negative AGC voltage to overcome the positive squelch control voltage at pin 2 of U1, causing that input to become negative, the output at pin 6 swings positive, causing the squelch gate to conduct and permitting the audio signal to pass through to audio amplifier U2. Thus, the receiver produces an audio output only for signals in excess of a certain average amplitude. This level, or threshold, is determined by the setting of R6 on the main chassis.

U2 amplifies the audio signal from squelch gate Q7. The output of U2 at pin 6 is coupled through R30 to the primary of T1. The secondary audio voltage is applied to board pins 21 and 22, and is then routed to the line audio terminals of J10 on the main chassis. The voltage at the output of U2 is also applied to a voltage doubler rectifier circuit comprising C11, R33, CR4, CR5,

R34, and C12. The rectified audio voltage is then applied to the front panel meter (M1 on yhe main chassis) through R35 and R36, as long as a near-ground potential from the receiver register is applied to the MTR input of the board (pin 18) permitting the base of Q9 to receive negative bias. The ground potential causer Q9 to conduct, causing Q8 to turn off. As long as Q8 remains off, the rectified audio voltage can be applied to the front panel meter. The meter can also be used, however, as a signal strength meter. In this case, the negative voltage at the MTR input of the board becomes positive, turning Q9 off and permitting Q8 to conduct. This in turn shorts the output of the rectifier circuit to ground and prevents any output from being applied to the front panel meter. The operation of the front panel meter as a signal strength indicator will be discussed in a subsequent paragraph.

The audio output from pin 6 of U2 is also coupled through R44 to board pin 20 (AUDIO). From pin 20, the audio signal is routed to a 10,000 ohm audio gain control potentiometer (R7) on the main chassis (Figure 7-33). The arm of the potentiometer is routed back to the PHONE AMPL INPUT (board pin 1) of the audio amplifier board. The signal is then applied through R27 to pin 2 of U3. U3 amplifies the signal, and couples its output at pin 6 through R32, C10, and C13 to board pin 19 (PHONES OUTPUT). From this point, the signal is routed to the headphone jack assembly (A28). Electrolytic capacitors C10 and C13 are connected "back-to-back" to provide high-capacitance ac blocking (a single electrolytic capacitor would not be suitable for handling the ac output of U3). Note that the audio gain control potentiometer (R7 on the main chassis) controls only the amplitude of the headphone output and has no effect on the amplitude of the audio line output signal.

4.3.2.11 Type 7899 Gain Control (A14). - Figure 7-16 is the schematic diagram of the gain control. The purpose of this circuit is to derive gain control voltage from the appropriate audio input, process this voltage to achieve the desired gain control characteristic, and apply the voltage to the gain controlled stages in the RF and IF sections of the receiver. Three gain control modes are available to the receiver operator: NORM AGC (normal automatic gain control), HOLD AGC (hold automatic gain control), and MAN (manual gain control). If the NORM AGC gain mode is selected, an AGC voltage with a fast-attack fast-decay characteristic is produced. This type of AGC characteristic is suitable for AM, FM, and CW reception. In addition, this gain mode is automatically selected whenever the receiver is operated in the ISB detection mode. The HOLD AGC gain mode is most suitable for LSB/USB reception, where a fast-attack delayed-decay characteristic is desired (a two second delay is provided, although the delay time may be changed). In the MAN gain mode, no signal-derived gain control voltage is produced. Instead, the gain control voltage (and hence the receiver gain) is set manually by the front panel RF GAIN control (the RF gain control also functions in the AGC gain modes).

A functional block diagram of the gain control is shown in Figure 4-5. Audio inputs from the AM, USB/CW, and LSB demodulators are applied to an electronic switch which selects the audio signal appropriate for the detection mode (for the FM detection mode, the AM demodulator input is utilized for AGC

purposes). Assuming that the NORM AGC gain mode has been chosen by the operator, the selected audio input is applied to a peak circuit which produces a voltage proportional to the peak signal input level. This voltage is then applied to a threshold circuit that permits automatic gain control action only for signals above a certain predetermined threshold (the AGC is thus "delayed", and does not act for weak signals below the threshold level). Both the input and output of the threshold stage are applied to the signal strength circuit which buffers the AGC voltage and drives the signal strength meter on the front panel if this mode of metering has been selected (the meter can also be used to indicate the line audio output power as previously described). The threshold stage also drives a gain control amplifier which provides gain control voltage to the appropriate receiver IF stages. The output of the gain control amplifier is applied to a second gain control amplifier as well. The output of this stage is then applied to the attenuator shaper (A2A1) for RF gain control.

In the HOLD AGC gain mode, operation of the gain control circuits is the same as described above. In addition, however, the digital control input to the time constant switch causes the time constant of the peak detector to increase. The peak of the audio input from the AM demodulator is stored by the hold timer circuit (regardless of the detection mode). When the signal level drops, the timing circuit is activated, and after the delay interval (normally two seconds) reverts the peak detector time constant back to its normal fast-decay characteristic via the time constant switch.

In the MAN gain mode, the digital control inputs cause the output of the threshold circuit to be shunted to ground. The receiver gain is then controlled exclusively by the manual gain circuitry.

Referring to Figure 7-16, the gain control inputs are the audio outputs from the AM demodulator, the USB/CW demodulator, and the LSB demodulator. The audio signals are applied to the inputs of digitally controlled electronic switches U1A and U1B, which select the appropriate audio input. The switches are activated by digital control inputs from the receiver register. U1B, for example, has the USB/CW and LSB audio inputs applied to B_0 (pin 2) and B_1 (pin 1), respectively. As long as the B control input (pin 10) is at ground potential, only the B_0 input will be internally coupled to the output at B_C (pin 15). If a positive voltage (from the receiver register) is applied to the LSB control input (board pin 16), that potential will be felt at the B control input of U1B, causing the device to prevent the B_0 input (USB/CW audio) from reaching the output at B_C. Instead, the B_1 input (LSB audio) is now internally coupled to B_C. U1B then, can be viewed essentially as an electronically controlled SPDT switch. With no voltage applied to B, B_0 is made to B_C, and when a positive voltage is applied to B, B_1 is made to B_C. The LSB/USB/CW output of U1B at B_C is applied to the A_1 input (pin 13) of U1A. The A_0 (pin 12) input receives the AM demodulator audio signal from board pin 19 (AM DETECTOR IN) through R5. U1A is identical to U1B. A positive control input at A (pin 11) from the receiver register causes A_1 to be internally coupled to A_C (pin 14), while a ground (or near ground) input at A results in A_0 being internally coupled to A_C.

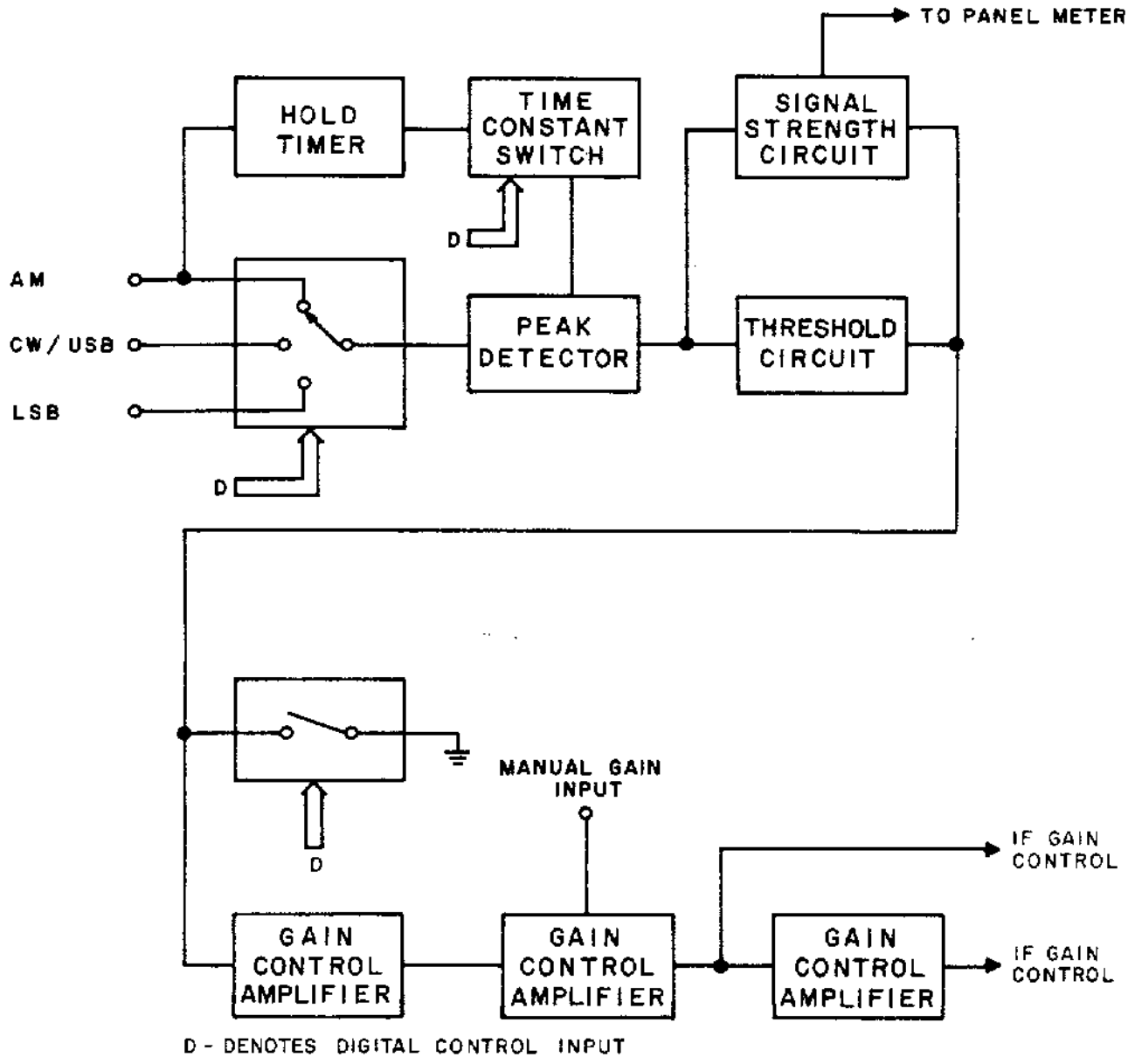


Figure 4-5. Functional Block Diagram, Gain Control (A14)

In the CW FIXED, CW VAR, USB, or ISB/USB detection modes, a positive potential is applied only to the A control input of U1A. As a consequence, U1A selects only the A_I input from B_C of U1B to be coupled to A_C. Since no positive voltage is applied to the B input of U1B, the USB/CW audio signal is coupled from B_O to B_C, then from B_C to A_I (via a hard-wire connection) and from A_I to A_C. Thus, only the desired USB/CW audio signal appears at the output of the electronic switch for application to the AGC circuitry. In the LSB or ISB/LSB detection modes, the receiver register causes both the A and B control inputs to become positive. As a consequence, the LSB audio signal (at board pin U) is coupled from B_I to B_C, from B_C to A_I, and from A_I to A_C. Thus, only the desired LSB audio input appears at the output of the electronic switch. In the AM detection mode, neither the A nor B control inputs are positive, with the result that only the desired AM audio signal appearing at A_O is coupled to A_C. In the FM mode of operation, the AM audio input is used for AGC purposes. As a result, operation of the gain control circuitry is identical for both the FM and AM detection modes. Figure 4-6 is a simplified illustration of the signal selection arrangement, substituting SPDT toggle switches for U1A and U1B.

The selected audio output at A_C is applied through R10 to the $\overline{\text{FM/ISB}}$ audio output (board pin 10) from where it is routed to the $\overline{\text{FM}}$ and $\overline{\text{ISB}}$ audio input of the audio amplifier (A13). Q2 is a transistor switch that is activated during the LSB, USB, or CW modes of operation. This switch causes R11 to shunt the $\overline{\text{FM/ISB}}$ audio output terminal, reducing the signal level applied to the audio amplifier (A13) for signal level equalization.

The audio output of U1A (pin 14), is applied to the base of amplifier Q4. The emitter output is dc coupled to the base of emitter follower Q5. The (positive) audio emitter output of Q5 charges C3 through R18. The voltage applied to pin 5 of U2A is proportional to the peak audio input to R18 and C3. R21 shunts series circuit R18 and C3 (through time constant switch U1C), assuming that the NORM AGC gain mode has been selected (the operation of the time constant switch in the various gain control modes will be discussed in a subsequent paragraph), resulting in a fast-attack fast-decay AGC characteristic. The positive AGC voltage is amplified and buffered by U2A, and applied through R71 and R75 to the non-inverting input (pin 3) of U2B. The output of U2B is applied to CR9. Since that diode passes only positive voltages to the subsequent circuitry, it is necessary that the voltage on the non-inverting input be more positive than the fixed voltage at the inverting input (pin 2). Otherwise, the output of U2B will be negative, reverse biasing CR9, and preventing AGC voltage from being passed to the next stage. The voltage applied to the inverting input is determined by R27, R30, and R34. As a result AGC action can only occur when the AGC voltage at the non-inverting input exceeds the positive threshold voltage at the inverting input. Thus, delayed AGC action is obtained, and receiver gain is not reduced for weak signals below a predetermined level (2 microvolts) as set by the threshold voltage applied to the inverting input of U2B. This threshold voltage can be reduced by shunting the threshold adjust terminal (board pin 11) to ground through an appropriate value of resistance.

The positive AGC voltage from CR9 is passed through R39 and R42 to the inverting input (pin 2) of U3B. Q9 is turned off in either AGC gain mode,

and therefore has no effect on AGC operation. The AGC output voltage of U3B at pin 1 is negative. CR10 forward biases if a positive voltage appears at pin 1 of U3B causing feedback resistor R47 to be shunted by a low resistance, decreasing the gain of U3B to a very low level. Thus, the output of U3B cannot go positive. R76 provides a small amount of bias for CR10 and the inverting input of U2.

The negative AGC voltage from U3B is applied through R73 to the base of emitter follower Q12. The negative emitter AGC voltage output is applied through R55 to the IF AGC output terminal (board pin 7), and is then applied to the gain-controlled stages in the 455 kHz IF amplifier (A8) and AM demodulator (A9), causing reduced gain in these stages.

In addition to being applied to the base of Q12, the negative AGC voltage from U4B is also applied through R51 to the emitter of voltage level shifter Q13. The voltage output level of Q13 can be adjusted by varying R74. This in turn sets the quiescent AGC output voltage of amplifier U4A. The amplified AGC output at pin 7 of U4A is applied through R62 to the RF AGC output terminal (board pin 4), and from there routed to the attenuator shaper (A2A1) for application to the PIN diode attenuator on the input converter (A2).

In the MAN gain mode, a positive voltage at board pin 12 (MAN) turns on Q6. As a result, Q7 and Q10 turn off. The positive potential at the collector of Q7 turns on Q9. Q9 shunts the positive AGC output voltage from pin 1 of U2B through CR9 and R39 to ground, preventing any further AGC action. The manual gain control voltage at board pin 8 (MANUAL GAIN INPUT) passes through R48, R46, and R43 to the inverting input (pin 2) of U4B. The operation of the subsequent gain control stages remains unchanged. However, they are no longer controlled by AGC voltage (from U2B), but instead by the output voltage from the RF GAIN potentiometer on the main chassis (Figure 7-33). A greater positive manual gain input voltage (caused by rotating the RF GAIN potentiometer counterclockwise) results in more gain reduction.

The RF GAIN control can also be used to reduce receiver gain in the AGC modes of operation. In either AGC mode, Q10 is turned on (by the receiver register via Q6 as described above) resulting in the bottom end of R69 being placed near ground potential. The voltage dividing action of R46 and R48 (in series), and R69 reduces the manual gain voltage that can be applied through R43 to the inverting input of U3B. If the RF GAIN control is fully clockwise, no manual gain voltage will be felt at the inverting input of U3B, and the AGC circuitry will exclusively control receiver gain. If the RF GAIN control is rotated counterclockwise, however, a positive voltage (dependent upon the RF GAIN control setting) will be applied to the inverting input of U3B, and reduce receiver gain as described above. Since the voltage dividing action of R69, R46, and R48 reduces the manual gain voltage that can be applied to the inverting input of U3B in the AGC modes of operation, only a limited degree of manual gain control can occur (during AGC operation). The receiver AGC will still be effective as long as the received signal is strong enough to produce a positive AGC voltage at the inverting input of U3B (from U2B) that exceeds the manual gain control voltage at that point as set by the RF GAIN control.

U1C is an electronic switch used to alter the time constant of the peak detector when the HOLD AGC gain mode is selected, and is identical to switches U1A and U1B previously described. If either the NORM AGC or MAN gain mode is selected, a positive voltage from the receiver register applied to board pins N (NAGC) or 12 (MAN), respectively, is routed to control input C of U1C, causing C_I to be internally connected to C_C, which is grounded. This results in R21 being effectively shunted across series circuit R18 and C3, providing the normal fast-attack fast-decay AGC characteristic. In the HOLD AGC gain mode, however, input C of U1C receives no positive input, but instead is held near ground potential. As a result, C_I is no longer internally connected to C_C. R21, therefore, no longer shunts series circuit R18 and C3, resulting in a much longer discharge time for that capacitor. C_O, however, is now internally connected to C_C, causing the connected end of R72 to be grounded. The effect of R72 is to reduce the output voltage of U2A applied to U2B compensate for the increased input voltage to that amplifier caused by R21 no longer being in shunt with C3. In the HOLD AGC gain mode, only a positive input from Q3 (via R1 and CR7) can cause U1C to revert to its previous state.

Time constant switch U1C is controlled by the hold timer circuit comprised of Darlington pair Q1-Q3 and the associated components. The hold timer uses the audio input voltage from the AM demodulator (board pin 19) as the basis for producing a dc level representing the peak amplitude of the input signal. This is accomplished by applying the (positive) audio input voltage from the AM demodulator through R4 to charge C1. The positive voltage across C1 and R7 turns on Q1 and Q3, resulting in a near-ground potential applied through R1 and CR7 to control input C of U1C. As a consequence, R21 is prevented from shunting C3 (as explained in the previous paragraph), resulting in a long AGC time constant. As the audio input signal drops, C1 discharges causing Q1 and Q3 to begin to shut off. Accordingly, the collector voltage of both transistors begins to rise, but the charging current of C2 through R7 and other shunt impedances apply a counteracting positive bias to the base of Q1, delaying the turn-off time of that transistor and Q2. When the transistors do turn off, the positive voltage at the collectors is applied to control input C of U1C, causing R21 to once again be switched in shunt with C3, producing the fast AGC decay characteristic. Thus, the hold timer circuit causes the AGC decay time constant to remain long for a fixed period of time (two seconds) after the signal level begins dropping, after which the AGC circuit reverts to its normal fast decay characteristic. By shunting additional capacitance across board pins W and V, the delay time can be increased.

U3A receives AGC voltage at its inverting input (pin 6), amplifies it, and sends it to the gain monitor and signal strength meter circuits. The input to U3A comes from the outputs of both peak detector amplifier U2A and threshold circuit amplifier U2B, provided that either the NORM AGC or HOLD AGC gain modes has been selected. Under weak signal conditions, the input to U3A comes entirely from U2A since U2B produces no output until the received signal level becomes strong enough to reach U2B's threshold. Since the collector of Q8 is near ground potential, R28 and R31 reduce the AGC voltage from the output

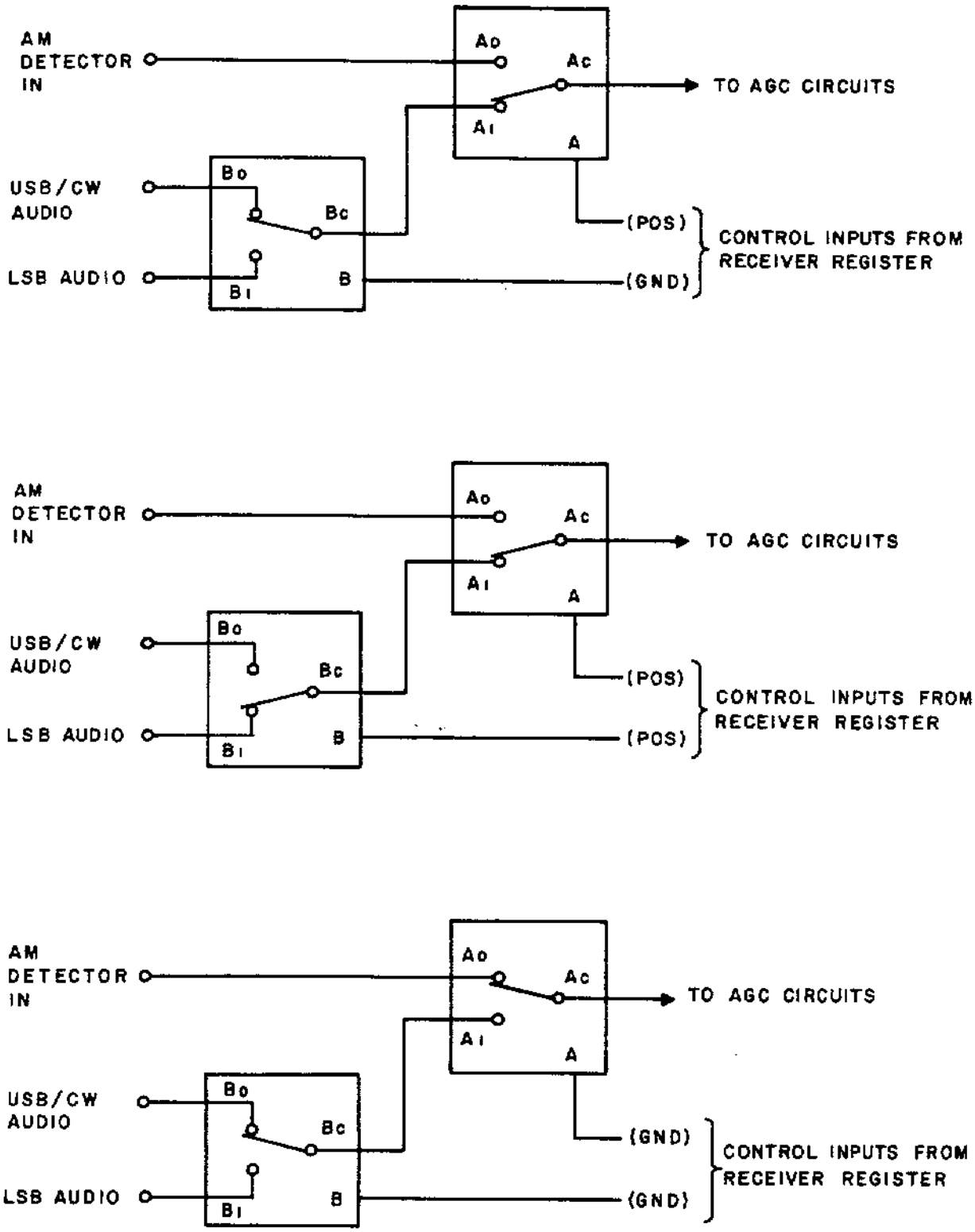


Figure 4-6. Simplified Functional Block Diagram of A14U1A and A14U1B

of U2A to the input of U3A. When the received signal becomes strong enough to cause the developed AGC voltage to exceed the threshold level of U2B, the AGC action results in a much slower increase in output voltage from U2A as the received signal level increases. The output of U2B, however, coupled to the inverting input of U3A through CR9, R39, and R36 begins to rise, causing the output of U3A to continue to increase negatively with an increase in received signal strength at approximately the same rate as it rose when the received input signal was below the AGC threshold level. As a result, the signal strength meter readings are not "compressed" for signal levels above the AGC threshold. In the MAN gain mode, a positive input from the receiver register at board pin 12 (MAN) causes Q6 to turn on, Q7 to turn off, Q8 to turn off, and Q9 to turn on. With Q8 off, more voltage from the output of peak detector amplifier U2A is passed to the input of U3A. At the same time, Q9 (now on) shunts the output of U2B (through CR9 and R39), preventing any developed AGC voltage from being applied to the inverting input of U3A. Thus, in the MAN gain mode, only the output of U2A is applied to U3A, as opposed to the NORM AGC and HOLD AGC gain modes where both the output of U2A and U2B are applied to the input of U3A. In any mode, the output of the gain monitor and signal strength circuits is proportional to the received signal strength.

The gain control board has two other features that are not utilized in a standard WJ-8888 Receiver. One of these features is an "AGC dump" circuit comprising Q14, Q15, R50, and R68. During normal operation, a ground potential at board pin D (AGC DUMP) causes Q14 to be cut off, which in turn cuts off Q15. The resulting high collector resistance of Q15 in parallel with time constant capacitor C3 has no appreciable effect on the AGC time constant, and the AGC circuit operates in its normal fashion. If a positive potential (a TTL logic "one" level), however, is applied to board pin D, Q14 and Q15 turn on. The resulting low collector resistance of Q15 rapidly discharges C3, and bring the gain control voltage to zero. The AGC dump feature is typically used in receivers that are remotely controlled in applications where the receiver must tune rapidly from one frequency to another (in such cases, any residual AGC voltage remaining on C3 will momentarily desensitize the receiver until the capacitor has discharged, thus hindering reception at the new tuned frequency).

The other feature is the DIVERSITY OUTPUT at board pin R. This output provides a positive output voltage proportional to the AGC voltage generated in the gain control circuitry. The diversity output is used when two or more receivers are employed to receive the same signal (at the same frequency), each using different antennas (i.e., diversity reception). In such a configuration, the receivers might all use a common AGC line. If the diversity output of each receiver is used to control the common AGC line simultaneously, then the receiver that is responding most strongly to the signal at the common tuned frequency will produce the largest diversity output voltage. The high AGC voltage thus produced will desensitize all other receivers (suppressing their background noise), resulting in audio output primarily from the receiver responding most strongly to the signal.

Neither the AGC DUMP nor the DIVERSITY OUTPUT board pin sockets are wired to any other connectors in the receiver. If it should become necessary to

have access to these terminals, they can be wired to the spare pins of J1 or J2.

The above gain control board circuit description applies to WJ-8888 Series Receivers with serial numbers 26-48, 71-88, and 90 up. Standard WJ-8888 Receivers and modified WJ-8888-( ) Receivers are numbered in the same sequence. Thus, no two WJ-8888 Series Receivers can have the same serial numbers.

The gain control board in receivers with serial numbers 1-25, 49-70, and 89 differ from the gain control board described above in the following respects:

(1) No AGC dump circuitry or diversity output is provided.

(2) The manual gain input circuitry is configured so that the RF GAIN potentiometer has no effect in the manual gain mode of operation.

(3) There are minor differences with regard to wiring and component values. The schematic for this board is not included with this manual as it has already been provided with the documentation that accompanied the receivers containing the board.

4.3.2.12 Type 791275 Phone Jack Assembly (A28). - Figure 7-31 is the schematic diagram for the phone jack assembly. A phone jack plugged into J1 interrupts the audio signal applied to the rear panel phone audio output connector (J10 pin 7).

4.3.2.13 Optional Type 791451 Logarithmic IF Amplifier Assembly (A7). - Figure 7-10 is the schematic diagram for the logarithmic IF amplifier assembly. This assembly receives its input from the 455 kHz IF filters and produces a demodulated output at J23 (located on the receiver rear panel) that is proporational to the logarithm of the amplitude of the 455 kHz input.

The input signal is applied to emitter follower Q1, which provides input isolation. Q1's output is amplified by tuned-collector amplifier Q2. R10 introduces degeneration into Q2's emitter circuit to improve linearity and signal handling capability. The output of Q2 is applied to emitter follower Q3, which steps down the circuit impedance to match the impedance presented by U1 and U2.

U2 is a logarithmic amplifier that uses two in-phase inputs to develop its logarithmic output. One of these inputs is applied directly to pin 4, and then to pin 7 through R20. The input signal is also applied to the non-inverting input of U1, which provides 35 dB of voltage gain. U1's output is then applied to pin 12 of U2. U2 processes the inputs (to provide the desired logarithmic characteristic), sums them, and provides a differential output to the primary of transformer T1.

The stepped-up secondary voltage is applied to emitter follower Q4. L2, CR1, R27, and C13 form a half-wave detector circuit that demodulates the signal output from the emitter of Q4. R28 provides a slight forward bias to hot-carrier diode CR1 to improve detection linearity. The demodulated signal output of the detector is then applied through R29 to the non-inverting input of U3. U3's output is applied through R37 to board pin 22 and then to J23 on the receiver rear panel.

R34 is used to adjust the quiescent dc output level of U3 to zero volts. Under strong signal conditions, the output voltage will rise in excess of +1 volt.

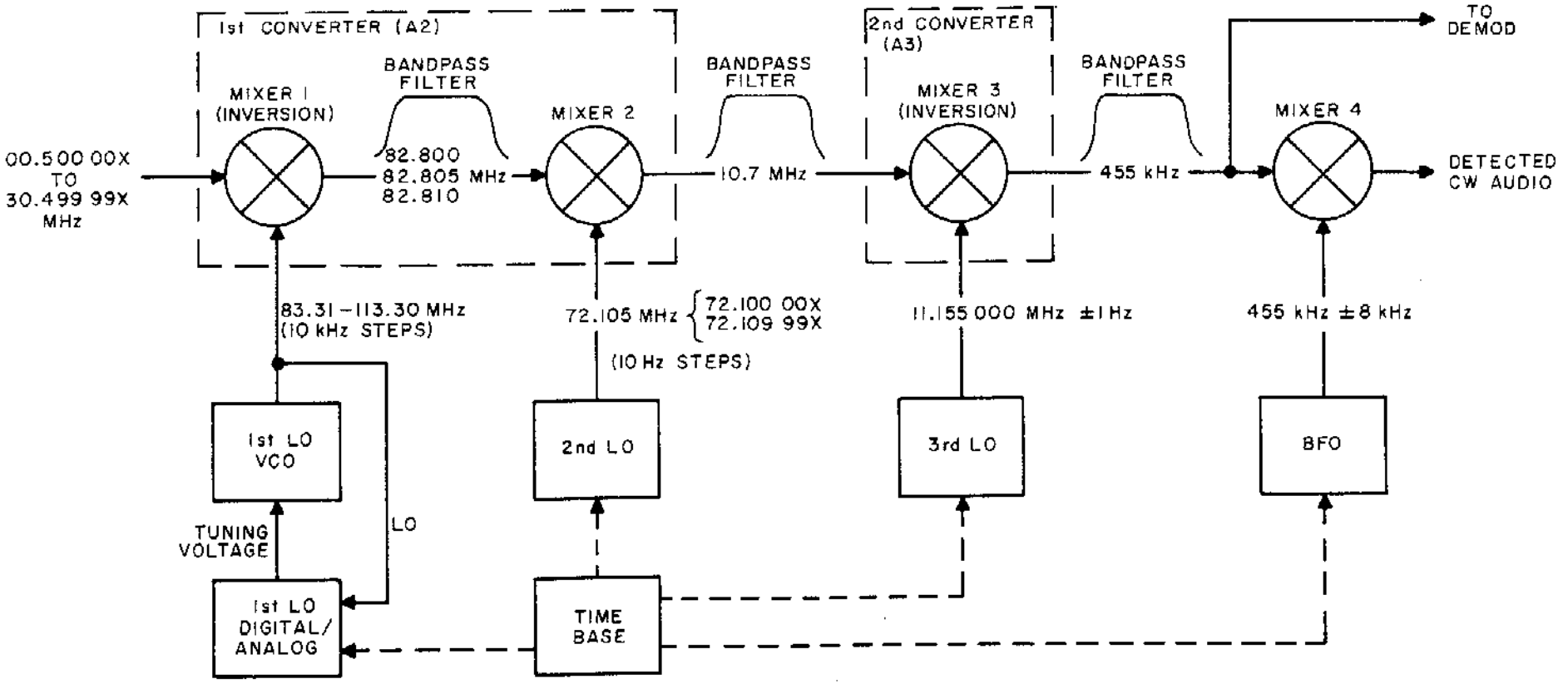


Figure 4-7. Frequency Synthesizers, Functional Relationships

4.4.1 SYNTHESIZERS RELATIONSHIPS. - Figure 4-7 shows the relationship of the synthesizers to the receiver signal processing. In essence, synthesizers provide three signals for translating the RF input signals to 455 kHz. The 455 kHz IF is then demodulated by other stages in the receiver. If the receiver operates in the BFO mode, a fourth synthesizer signal beats with the 455 kHz IF to produce an audio output. The actual tuning process involves the 1st LO and the 2nd LO.

NOTE

Throughout the synthesizer discussions, an x in frequency references indicates the unused 1 Hertz digit (i.e., 29.999 99x MHz).

The 1st LO tunes from 83.31 MHz to 113.30 MHz in 10 kHz steps. This range corresponds to an RF input range of 0.5 MHz to 30.499 99x MHz. All RF signals convert first to signals in a 10 kHz range from 82.810 to 82.800 MHz. A filter following the 1st mixer limits the converted signals to a total range of 82.800 MHz to 82.810 MHz. This 10 kHz range is applied to the 2nd mixer, which then converts the 82.805 signals to 10.7 MHz.

The 2nd LO tunes from 72.109 99x MHz to 72.100 00x MHz in 10 Hz steps. This 9.99 kHz range provides translation of signals to 10.7 MHz. A bandpass filter following the 2nd mixer limits the signal range to 250 kHz.

The 3rd LO provides 11.155 MHz to the 3rd mixer. Signals centered on 10.7 MHz beat with the 3rd LO to produce signals centered on 455 kHz. The 455 kHz signals are either demodulated by other stages or are routed to the fourth mixer. A 455 kHz BFO signal from the synthesizer beats with the 455 kHz IF to produce an audio output.

All four synthesizer stages are referenced to a common time base. Signal inversion occuring in mixer 1 is reversed by inversion in mixer 3.

Table 4-2 shows translation frequencies for a 10 kHz segment of the receiver tuning range. Column B is tabulated for an input frequency of 0.500 MHz. Columns C and D are tabulated for input frequencies of 0.505 and 0.509 99x MHz, respectively. This 10 kHz range is the lowest tuning segment for the receiver. Any signal in this range is converted to a 1st IF frequency of 82.800 to 82.810 MHz. This is shown in columns B, C, and D for mixer 1. Furthermore, if the receiver is tuned higher than 00.509 99x MHz, the 1st LO will step to the next higher LO frequency, 83.32 MHz. This will, in turn, convert the signals in that 10 kHz portion of the RF tuning range to a 1st IF frequency. This continues in 10 kHz segments up the band to the maximum RF tuned frequency of 30.499 99x MHz. Any signal in the range of 0.500 to 30.499 99x MHz is converted to a 1st IF frequency in the range of 82.800 to 82.810 MHz. The 1st LO frequency corresponding to 29.999 99x MHz is 112.81 MHz.

Mixer 2 translates signals in the 1st IF range to the 2nd IF frequency of 10.7 MHz. To do this, the 2nd LO steps in 10 Hertz increments from 72.100 00x to 72.109 99x MHz. The 9.99 kHz range of the 2nd LO matches the increment sizes of the 1st LO, thereby providing for conversion of all RF signals to 10.7

Table 4-2. 1st And 2nd LO 10 kHz Tuning Increment

10 kHz Tuning Increment for 00.500 00x to 0.509 99x MHz

	A	B (0.500 MHz)	C (0.505 MHz)	D (0.509 99x MHz)	
MIXER 1	1st LO	83.310 00x	83.310 00x	83.310 00x	INVERSION
	RF INPUT	-00.500 00x	- 0.505 00x	-00.509 99x	
	1st IF	82.810 00x	82.805 00x	82.800 01x	
MIXER 2	1st IF	82.810 00x	82.805 00x	82.800 01x	
	2nd LO	-72.109 99x	-72.105 00x	-72.100 00x	
	2nd IF	10.700 01x	10.700 00x	10.700 01x	
MIXER 3	3rd IF		11.155 00x -10.700 00x 0.455 00x		INVERSION
			OR		
MIXER 4	3rd IF		0.455		
	BFO		0.455 ± 8 kHz		
			± 8 kHz audio		

DEMODULATION

Table 4-3. 1st And 2nd LO Frequencies Versus Tuned Frequency

To Obtain 1st and 2nd LO Frequencies for any Tuned Frequency
(00.500 00x to 30.499 99x)

TO OBTAIN 1st LO FREQUENCY	TO OBTAIN 2nd LO FREQUENCY
Drop 3 Least Significant Digits From Readout	Use 3 Least Significant Digits From Readout
15.756 35x	00.006 35x
Add 82.81 to the Remaining Digits	Subtract Them From
15.75 Add 82.81 98.56 = 1st LO Frequency	72.109 99x Sub. .006 35x 72.103 64x = 2nd LO Frequency

NOTE: X Indicates Unused 1 Hertz Digit

MHz. To determine 1st LO and 2nd LO frequencies corresponding to a receiver tuned frequency, refer to the example given in Table 4-3.

Mixer 3 translates the 10.7 MHz 2nd IF to 455 kHz. A fixed 3rd LO frequency of 11.155 MHz provides the necessary difference frequency for this translation.

Demodulation of the 3rd IF takes place in other stages of the receiver or in mixer 4 when the BFO mode is used. The BFO portion of the synthesizer varies a minimum of ± 8 kHz thus providing full pitch control for monitoring.

4.4.2 PHASELOCK LOOPS. - A phase lock loop consists of three basic components: a phase detector, a low-pass filter, and a voltage controlled oscillator. Figure 4-8 also shown an additional feature, a programmable divide-by-N stage. For now, assume this stage divides-by-1.

Output from the voltage controlled oscillator provides one input of the phase comparator with a signal. The other input to the phase comparator is a highly-stable, fixed-frequency reference source. If any difference exists between the two phase detector inputs, an error voltage drives the VCO to the same frequency as the reference input. A 1-kHz reference input means the VCO would be maintained at 1-kHz.

Dividing the VCO output by 2 before applying it to the phase detector results in an error voltage that drives the VCO to twice the reference frequency. A divide-by-3 action results in an error voltage that drives the VCO to 3-times the reference frequency. From this, the following relationship can be given: $F_{VCO} = N\ (F_{REF})$. Changing the divide ratio, N, causes the VCO frequency to change by a factor of N times the reference frequency. The least possible change in VCO frequency then, corresponds to the reference frequency supplied to the phase detector.

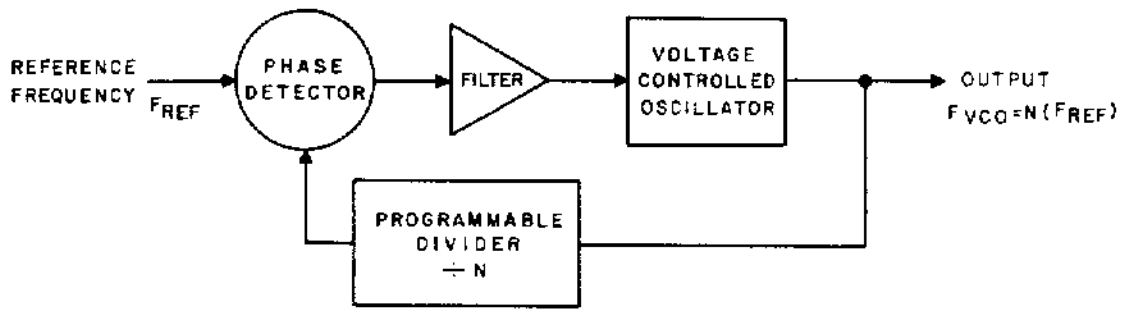


Figure 4-8. Basic Phase Lock Loop

Phase detectors used in these synthesizers provide positive and negative pulses, related to the direction of the error, as an indication of a frequency difference at their inputs. The greater the error, the wider the pulses.

Integration in the filter varies the voltage supplied to the voltage controlled oscillator. This drives the frequency in the correct direction to reduce the dif-

ference between the phase detector inputs. Under lock conditions, the phase detector provides extremely narrow positive and negative pulses to the filter, thereby maintaining the voltage controlled oscillator at the desired frequency. In actuality, the loop is never truly locked, for the phase detector always provides correction pulses to the filter.

4.4.3 1st LO SYNTHESIZER. - The 1st LO tunes from 83.31 MHz to 113.30 MHz in steps of 10 kHz. This corresponds to a receiver tuning range of 00.500 00x MHz to 30.499 99x MHz. Figure 4-9 shows a functional drawing of the 1st LO devoted primarily to the divide-by-N portion of the loop.

When the loop is locked, the VCO frequency is divided down to 10 kHz by the counters. Phase detector U15A compares this signal with a 10 kHz reference from the time base stages, and produces an error voltage if the two inputs are out-of-phase. This changes the VCO tuning voltage which makes a slight correction to the frequency, thereby maintaining the VCO frequency in-lock with the 10 kHz reference. To shift the VCO frequency, the divide-by-N is changed to a new ratio. This causes the 10 kHz signal to the phase detector to be off-frequency, so the phase detector and integrator produce an error voltage driving the VCO to the frequency which divides down to 10 kHz.

Divide-by-N stages must give a 10 kHz output for all input signals in the range of 83.31 to 113.30 MHz. To do this, they must provide a divide ratio of 8331 to 11 330 thereby covering all possible input frequencies to 10 kHz. The basic divide capability of these stages is 16 000. That is, U5, U10, and U13 each provide a divide-by-10 action. U14 is a divide-by-16 stage. (10 x 10 x 10 x 16 equals 16 000). For this divide ratio the input frequency would have to be 160 MHz for an output frequency of 10 kHz. Because the VCO operated in the range of 83.31 MHz to 113.30 MHz, the basic counter stages must be modified.

Preventing them from counting down the entire 16 000 counts is one method used. If the offsets shown connected to the counters stopped the count at 7719, there would be 8281 decrements (16 000 minus 8281 equals 7719). With offsets in the circuit then, the VCO would maintain a frequency of 82.81 MHz which corresponds to a tuned frequency of 00.000 00x MHz. Because the receiver only tunes as low as 00.500 00x MHz a method is needed to increase the count by at least 500.

The maximum count increase is required when 113.30 MHz must be divided down to 10 kHz. This would require a maximum divide ratio of 11 330. To increase the divide ratio to 11 330 requires an additional divide ratio of 3049. (8281 plus 3049 equals 11 330).

To gain these additional 3049 counts, the four counters start their sequence not from 16 000, but instead from 3049. Thus U14, the most significant digit, is loaded with a 3, U13 with a 0, U10 with a 4, and U5 with a 9. Now the count sequence is 3049, 3048, 3047, ... 0039, 0029, 0019, 0009, 15 999, 15 989, ... 7739, 7729, 7719 = terminal count. At count 7719, a pulse would be provided to the phase comparator and the counting chain recycles. Figure 4-10 shows count range. The terminal count pulse and recycling occurs at a 10 kHz rate.

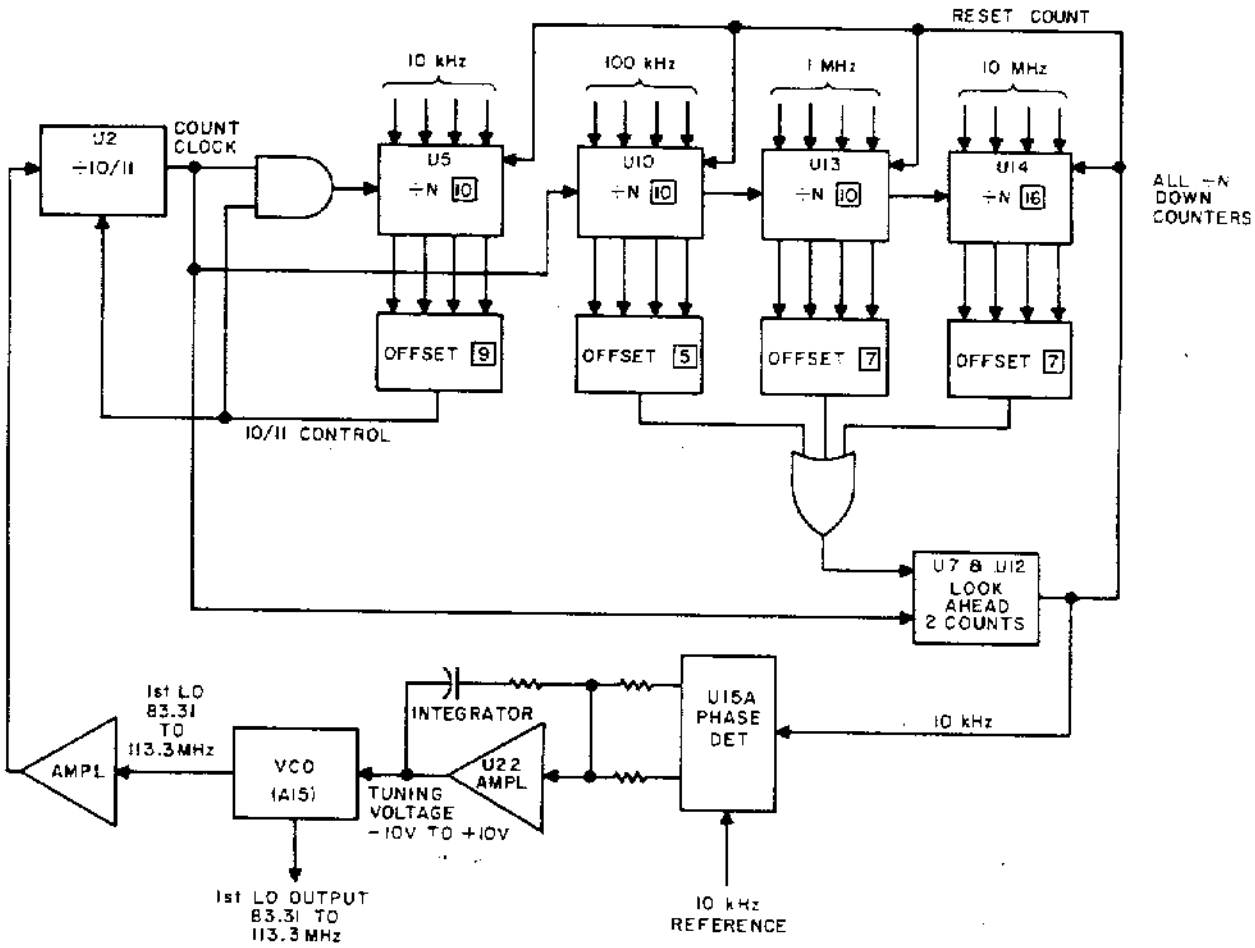


Figure 4-9. 1st LO Functional Block Diagram

So far the divide action description neglected actual circuit operations and practical considerations. For example, two clock pulses are lost because U5 and U10 are decremented together by the clock, and there is no borrow from U10. The effect of this is to change the terminal count from 7719 to 7739. Another problem, the counters cannot be reset at terminal count without losing clock pulses. To overcome this, a look ahead stage is added which performs the last two count operations while the counters are being reset. When a count of 7759 is reached, the look ahead circuit activates the cross-coupled NAND stages and they complete the last two pulses of the cycle.

Table 4-4 shows an assumed number of 2436 worked down to the actual terminal count of 7739. Knowing both the actual terminal count (7739) and the number loaded into the counters (2436) allows calculation of the total pulses required to decrement the counters to terminal count. If the two borrow counts lost are disregarded, then 2436 pulses are required to decrement the counters to 0000 (this corresponds to 16 000). If the counters were loaded with zeros, this would be the start count for the count chain.

FIGURE 4-10 WJ-8888

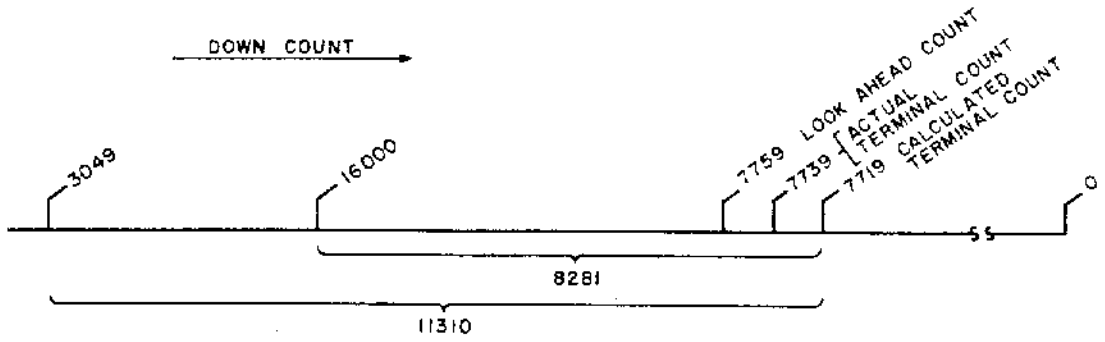


Figure 4-10. 1st LO Divide-By-N Range

The calculated terminal count is 7719. This means the counters start from an effective count of 16 000, and decrement down 8281 times to reach 7719. (16 000 minus 8281 = 7719.) To compensate for the two lost borrow counts at the 0-to-9 transitions of U5, the actual terminal count is made on 7739 instead of 7719. The net effect provides the required number of counts.

With the counters at 2436, 11 pulses to U2 are required to produce an output pulse. Note that a single output pulse from the prescaler decrements both U5 and U10. This results because U5 and U10 are connected in parallel and both receive the clock pulse from the prescaler.

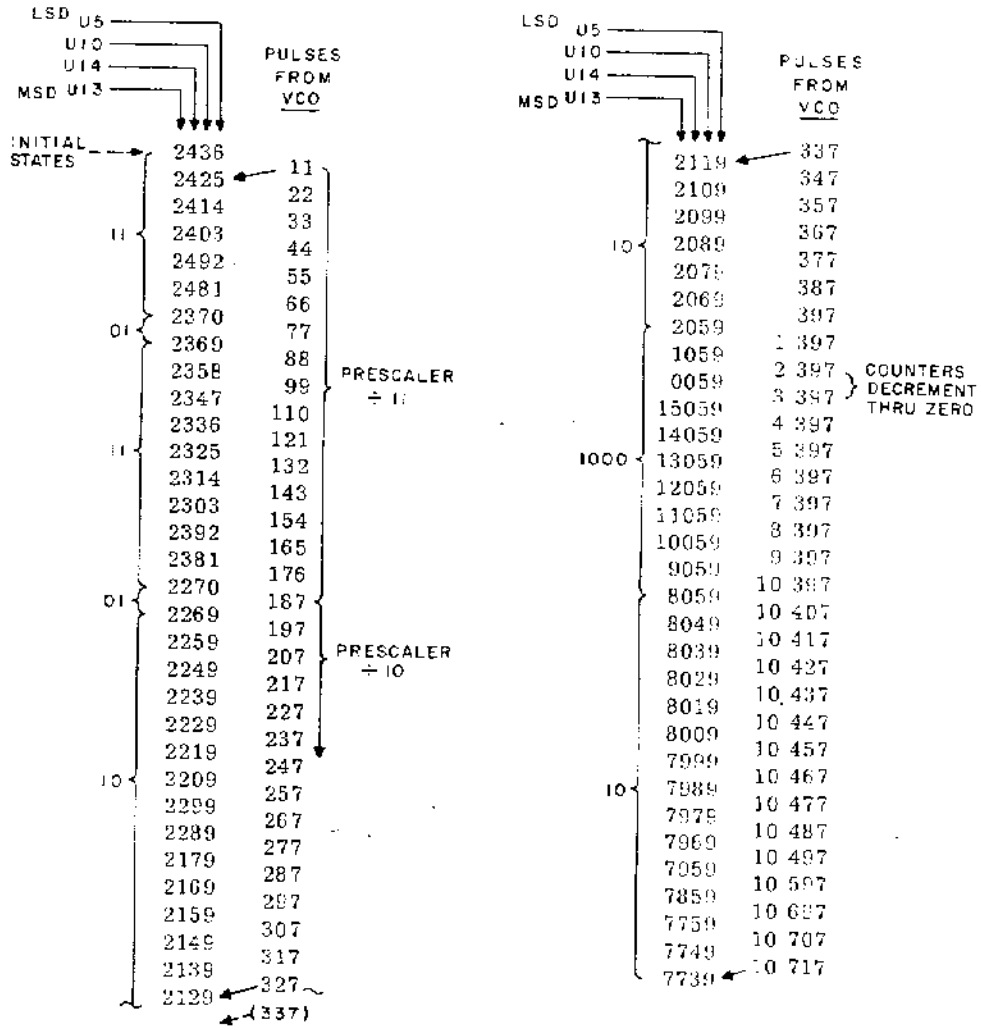
As the prescaler continues to divide-by-11, both U5 and U10 decrement one state for each pulse they receive and the count becomes 11 less each time. However, at the transition from 2370 to 2369, the count becomes only one less. In effect, a borrow is missed which should decrement U10 to state 5. If the borrow took place, the dividers would be at 2359.

As the prescaler continues to divide-by-11, the count works down to 2370, then 2369, when another borrow is missed. On this zero-to-nine transition of U5, the prescaler is converted to divide-by-10 and remains in that mode until terminal count 7739, when it reverts to divide-by-11 and a new cycle begins. When the prescaler is converted to divide-by-10 at the second 0 to 9 transition, counter U5 does not decrement again. It stays at state 9 until being reloaded for the next count sequence. To compensate for the two borrows missed from U10, the terminal count is made on 7739 instead of 7719.

Divide-By-N Integrated Circuit Data. - Refer to Figure 4-11 for pin designations and truth tables of these integrated circuits.

Dual modulo prescaler U2 operates at the upper frequency limit of 113.30 MHz. It is an emitter coupled logic device, so level translation is required for the inputs and outputs to work with TTL stages. It accepts the clock pulses from the VCO and maintains output Q low for 5 of the pulses and high for the subsequent 5 or 6 incoming pulses, depending on the state at $\overline{PE}$ pin 2. If pin 2 is low before the rising edge of Q, then Q will stay high for 6 more incoming

Table 4-4. 1st LO Decremented to Terminal Count



clock pulses and a divide-by-11 action results. Conversely, if $\overline{PE}$ is high before the rising edge of Q, then it stays high for only 5 more incoming pulses, and a divide-by-10 action results.

U5, U10, U13, and U14 are TTL down counters. U14 decrements from 0 to 15 and down through 0. The others decrement from 0 to 9 and down through 0. Otherwise they are all the same. These counters decrement on the positive going edge of the clock pulse. The buss output goes high in the 0 state and remains there until the leading edge of the clock pulse produces the transition to 9 (or 15). A low state applied to the $\overline{PE}$ input enables P0 thru P3. These inputs are independent of the logic level of the clock. Entering a number to the P0 thru P3 inputs causes the counter to begin its count at that number. However, until $\overline{PE}$ goes low again, the counter decrements through its normal sequence and does not reset to the number applied to the P inputs.

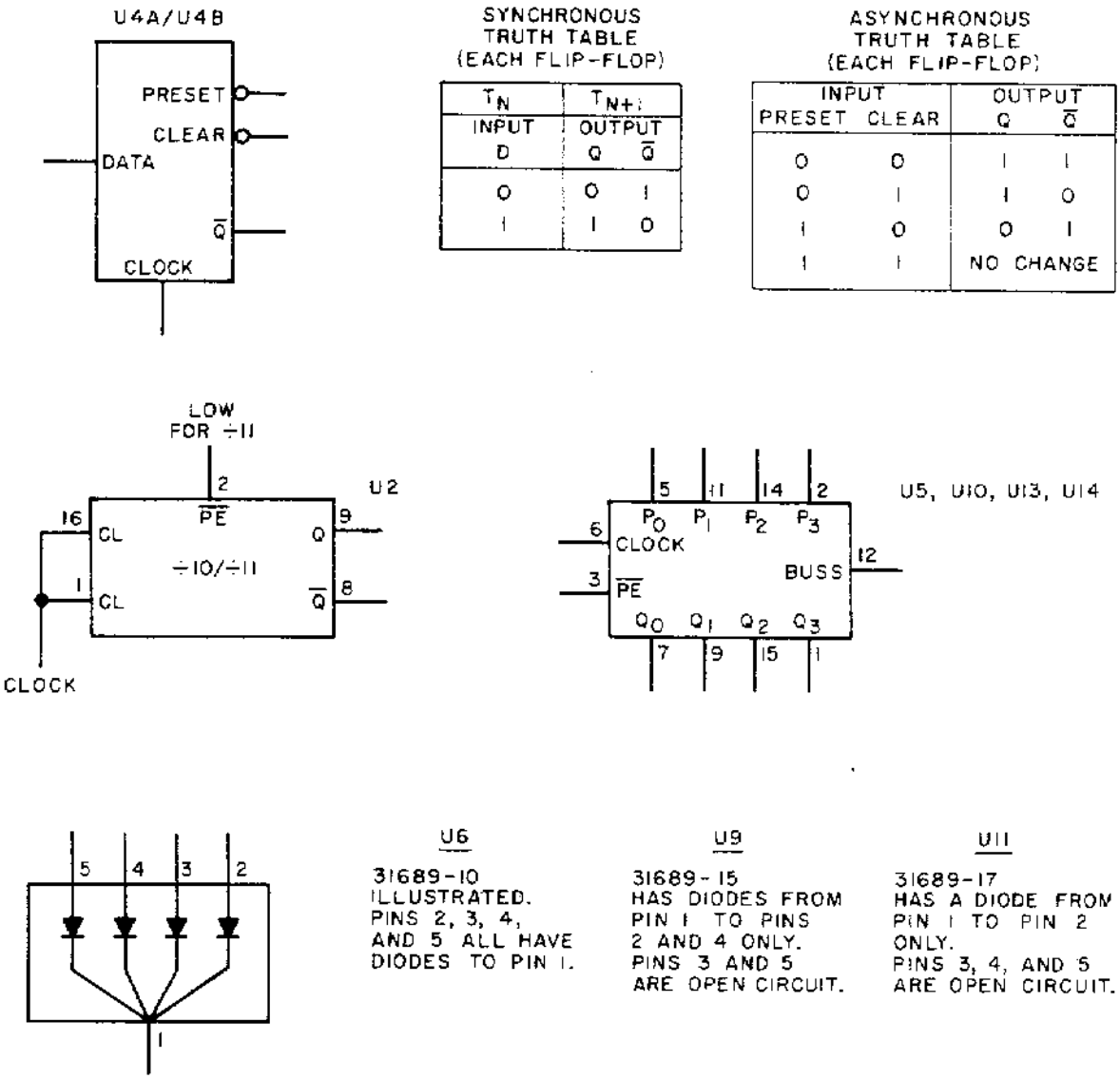


Figure 4-11. 1st LO Divide-By-N Integrated Circuits

U4 is a dual D-type edge triggered flip-flop. Information on the data input is transferred to the Q outputs on the positive-going edge of the clock pulse. This transfer is a function of level and is not directly related to transition time of the leading edge. When the clock is either high or low, the data input has no effect. A low input to the preset sets the Q output high. A low input to the clear input sets the Q output low.

Modules U6, U9, and U11 contain diodes connected from pin 11 to certain other pins depending on the dash number of the module. For the exact arrangement, refer to Figure 4-11.

Divide-By-N. - A general discussion of the 1st LO operation appeared in the functional description. These paragraphs describe the circuits in detail.

Count Sequence. - From the functional discussion remember that the counter chain has a basic count capability of 8281. This corresponds to a frequency of 82.81 MHz, (which is actually below the minimum required VCO frequency of 83.31 MHz). To establish any frequency above 82.81 MHz then, requires increasing the count capability by loading in the required amount to the P0 through P3 inputs of the four counters.

For example, if a VCO frequency of 107.17 MHz were required (24.360 00 MHz tuned), then a count of 10 717 would have to be established to produce a 10 kHz output. Knowing that we have a built-in count of 8281 allows calculation of the required number to be loaded in. That is, 10 717 minus 8281 equals 2436. For this discussion, assume that 2436 has just been loaded into the counters at the terminal count. (U14 with a 2, U13 a 4, U10 a 3, and U5 a 6.) Refer to Figure 7-20 for the schematic diagram of the 1st LO.

Terminal count resets the count chain in readiness for the first clock pulse of the new count sequence. The terminal count originates at the output of NAND U12C. As the output goes high, the chain is ready for the next pulse. Refer to later paragraphs for detailed explanations of the look ahead features associated with the cross-coupled NAND gates.

With the counters in initial states of 2436, U2 receives 11 clock pulses and produces its terminal count. The terminal count pulse is applied to differential amplifier Q1-Q2 which then supplies the pulse to NANDs U7B and U3A. They apply the pulse to counters U5 and U10, which both decrement one state. Table 4-4 shows the new count of 2625 after the 11 input clock pulses. For each succeeding 11 input pulses to U2, U5 and U10 each decrement 1 state, and the total count is reduced each time by 11.

However, notice that at the transition from 2370 to 2369, the count reduction is only 1. In effect, a borrow pulse to U10 is missing. This occurs again at the transition from 2270 to 2269. Remember in the functional description, mention was made that the terminal count of 7719 was theoretical and that in fact a real terminal count of 7739 was used. The loss of two borrow pulses to U10 accounts for using 7739 as the terminal count. Because counter U5 only passes through a 0 to 9 transition twice for any count sequence, the terminal count is always 7739.

Prescaler U2 changes to divide-by-10 when U5 decrements from 0 to 9 at 2270/2269. Also, U5 stops decrementing at this state 9. This means that only the 3 most significant digits continue to decrement to terminal count. U2 remains in a divide-by-10 condition for the remainder of the count cycle until being reset to divide-by-11 at terminal count, 7739.

Counters U2, U10, U13, and U14 then operate as conventional ripple counters, with the clock pulse for each counter taken from the Q3 output of the next most significant digit. From 2269, they decrement down to 0000 (effectively 16 000), 15 999, etc., and on down to the look ahead count of 7759. At 7759 the look ahead stage takes over. NANDs U7 and U12 make the last two counts, providing both a low for the $\overline{PE}$ line and an output pulse for the phase detector. Refer to the look-ahead paragraphs for an explanation of the exact sequence of these circuits.

Look Ahead. - The counters cannot be reset fast enough at terminal count to not lose clock pulses at the beginning of the next cycle. Therefore, a state is sensed 2 counts before the actual terminal count and NANDs U7 and U12 make the last two counts. During these two clock pulses the counters are reset and a terminal count is provided to the phase detector.

The terminal count number is 7739. For a two-count look ahead, the counters must activate NAND U7 on a count of 7759. To do this inputs 9 and 11 of U7C must be high. To obtain these conditions U14 must be a 7, U13 a 7, U10 a 5, and U5 a 9. Note that the 9 state for U5 was established near the beginning of the decrementing sequence.

For U14 a 7 state means that the buss line is low, pin 1 is low, and pins 15, 7, and 9 are high. A 7 is the only state for which this will be true.

For U13, a 7 also must be sensed. To do this, module U11 contains a diode connected from pin 1 to pin 2, the cathode being connected to pin 1. As U13 counts down, 7 is the first state reached where a 0 appears on that output.

For U10, a 5 is sensed. This means that module U9 has diodes connected from pin 1 to pins 2 and 4. Cathodes are connected to pin 1. As U10 decrements, 5 is the first state reached with 0's on Q1 and Q3.

For U5 an effective 9 is sensed; however, that action is an intergral part of the prescaler circuit so it will not be discussed here. Also, that 9 is sensed near the beginning of the count sequence when the prescaler changes to divide-by-10. The others are sensed near the end of the count sequence.

Returning to U14, the highest number to be loaded into it will be a 3. Remember that the maximum number of additional states needed to be loaded into the counters to provide the highest VCO frequency of 113.3 MHz is 3040 (8281 + 3040 = 11 330). In fact, pins BL and BN of the circuit board are hard wired to ground, as can be seen on the main chassis schematic. Loading the counters with some number, again say 2436, and working the count down, will serve to explain operation of the look-ahead terminal count.

The counters decrement from the assumed states of 2436 through 0000 (effectively 16 000), and then continue decrementing to look ahead count 7759. The actual sequence of obtaining the look ahead number is as follows. The least significant digit, a 9, occurres first, near the beginning of the decrementing sequence. The next counter to reach its look-ahead terminal-count number is most significant digit U14. As it reaches state 7 (1110), CR2, CR3, and CR4 put a high on pin 9 of NAND U7C. Also notice that diode CR5 then has a low on its anode. Thus it does not contribute current to R40, which would hold pin 9 of U3C high. Pin 9 does not drop low though until the other two counters reach their look ahead numbers.

Next U13 decrements to its look ahead state, also a 7. This puts a low on its Q3 output, which had been helping to keep a high on pin 9 of U3C.

Now only U10 needs to decrement to its preset number to allow NAND U3C to enable NANDs U7 and U12. When U10 decrements to a 5 state, its Q3 and Q1 outputs both go low and do not draw current through R40. This allows pin 9 of NAND U3C to drop low and its output goes high.

That high is applied to pin 11 of U7C. Pin 9 had previously been made high when U14 reached state 7. The counters are then at a count of 7759. The last two clock pulses corresponding to a decrement to states 7749 and 7739 are processed by NAND gates U7 and U12. Refer to the next paragraph for an explanation of this circuit.

NAND Terminal Count Completion. - Refer to Figure 4-12 for a redrawn view of the cross-coupled NAND gates. Included with the figure are a truth table and a timing diagram. When considering inputs R1 and S1, be sure to treat them as the total function of all inputs.

The leading edge at count 7759 has just decremented the counters from 7769 to 7759. This drops zeros through to NAND U3C (after propogation delay), which puts a high on pin 9 of U7C. This initiates the two count sequence of the cross-coupled NAND gates.

Considering R1, it goes high after the preset number is reached and stays high until the counters receive a low on their $\overline{PE}$ inputs. This takes away terminal count states holding pin 9 high. Propagation delay for counter U10 decrementing from a 6 state to a 5 state results in R1 going high some time after the 7759th clock pulse decremented the divider. However, when the dividers receive the low on their $\overline{PE}$ inputs, information on their P inputs appears at the Q outputs much faster than when the clock decrements the divider.

Input S1 normally clocks Q2 because Q1 and $\overline{Q2}$ maintain high states on the other two inputs. Outputs Q1 and Q2, though, do not change state because S1 is held low until look-ahead state 7759 is reached. When $\overline{Q2}$ goes high at the end of the two count sequence, S1 again clocks $\overline{Q2}$.

Output Q1 goes low when the look-ahead count propagates through to R1. When the counters get reset by a low state to their $\overline{PE}$ input, R1 goes low, and Q1 goes high.

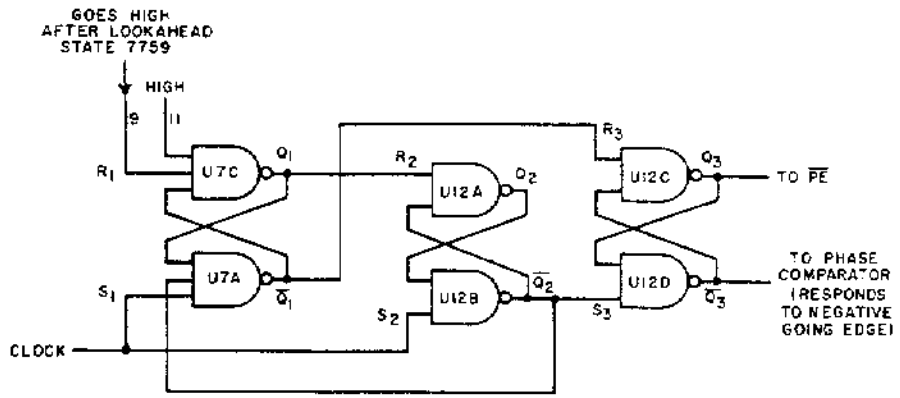
Output $\overline{Q1}$ normally changes state with the clock because S1 is enabled. When the look-ahead count is reached, S1 goes low and stays there until the end of the two count sequence when S1 begins to clock $\overline{Q1}$ again.

Input R2 maintains the same waveform as Q1 because they are wired together. S2 receives the clock. Output Q2 normally stays low because R2 (Q1) is held high. Only after the look-ahead count propagates through to R1 does Q2 go high. It stays high when R2 goes high because that is a latch condition. When S2 goes low again, Q2 and $\overline{Q2}$ change to low and high, respectively, and remain there because the clock high on S2 merely provides a latch condition.

Inputs R3 and S3 being physically wired to $\overline{Q1}$ and $\overline{Q2}$, maintains the corresponding waveforms. As long as S3 is held high by $\overline{Q2}$, the Q3 and $\overline{Q3}$ outputs stay high and low, respectively. When R3 ($\overline{Q1}$) is held high, and S3 ($\overline{Q2}$) drops low, the Q3 outputs change state. When S3 goes high, a latch condition exists and the Q outputs stay the same. Only when R3 (Q1) drops low do they again revert to Q3 high and $\overline{Q3}$ low. After that, R3 clocking high provides a latch condition, and the outputs do not change.

TRUTH TABLE

INPUTS		OUTPUTS	
R	S	Q	$\overline{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	LATCH	



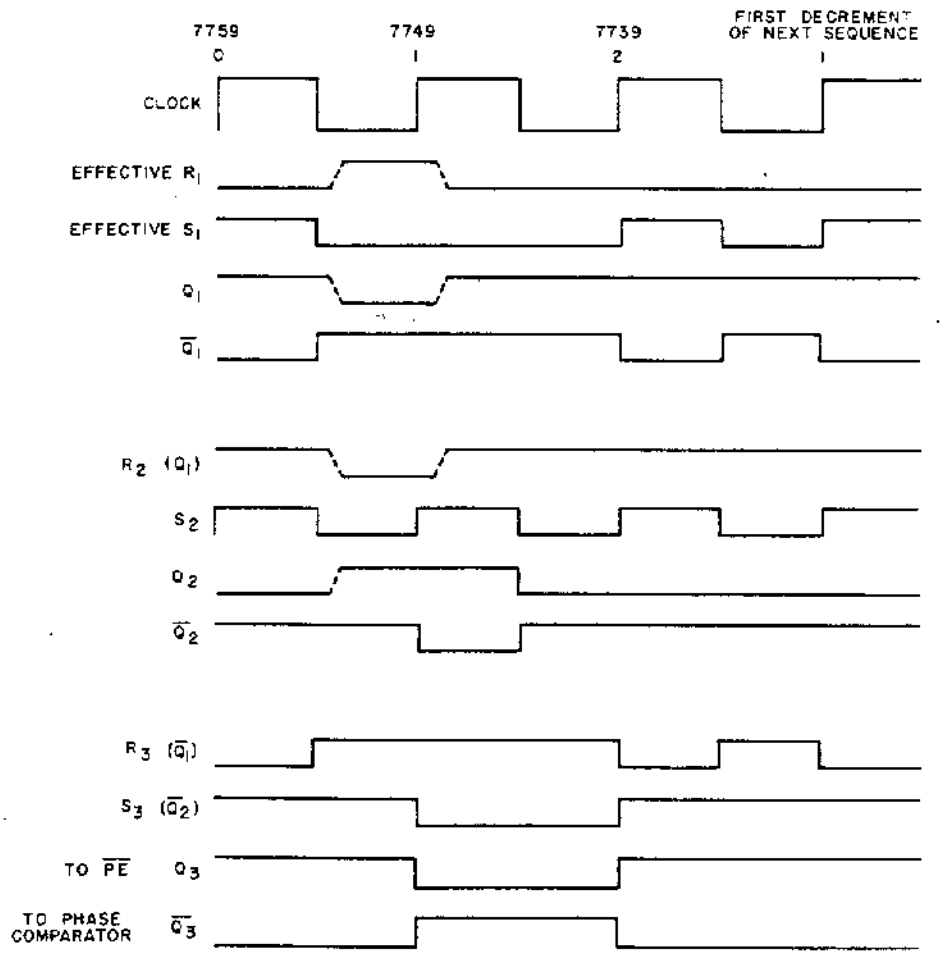


Figure 4-12. 1st LO NAND Terminal Count Sequence

The negative going (falling) edge of Q3 provides the phase comparator with an active low-going edge from the divide-by-N stages. When Q3 goes low for the one clock pulse from 7749 to 7739, the dividers are reset.

Prescaler Control U5. - This discussion assumes the $\overline{PE}$ line has just reset the counting chain, and that 0's were loaded into P0 through P3 of U5.

The low on the $\overline{PE}$ line made U4A $\overline{Q}$ high and U4B $\overline{Q}$ low. This results from the one receiving a low on its clear input and the other on its reset input. The $\overline{Q}$ from U4B keeps the output of NAND U3D high and also puts prescaler U2 in the divide-by-11 condition.

Inputs 3, 4, and 5 of NAND U7B are high. This makes output pin 6 low. Conditions making pin 3 high are as follows: With U2 having just received a low to its $\overline{PE}$ input, pin 2, its Q output is high and $\overline{Q}$ output is low. Differential amplifier Q1-Q2, then, has Q2 in the conducting state and voltage developes across R38. This voltage is the high state for pin 3 of NAND U7B.

When $\overline{Q}$ on U2 goes high, the output of NAND U7B goes low. This falling edge does not increment U5. As $\overline{Q}$ goes low the output of U7B then goes high and decrements counter U5.

The same pulse clocks flip-flop U4B, but the high on its data input keeps $\overline{Q}$ low. When counter U5 makes its 0-to-9 transition, however, flip-flop U4A changes it $\overline{Q}$ output from high to low. Remember that with U5 in its 0 state, the buss line was high and the Q outputs were low. On the 0-to-9 transition, Q3 goes high which clocks flip-flop U4A. The buss line does not drop low instantly because of the time constant of R26 and C40. This keeps the data input high long enough for Q3 to clock the flip-flop thus forcing $\overline{Q}$ low.

Module U6 contains four diodes which sense a zero. When combined with U4 this gives a look ahead state of 9. The cathodes all connect to pin 1. Anodes connect to pins 2, 3, 4, and 5. With any Q output of U5 high, current drawn through R39 developes a voltage which keeps the data input of flip-flop U4B high. Zero is the only state for which all Q outputs are low.

If the counter was loaded with 0's, the data input of U4B would be low. To prevent this the $\overline{Q}$ output of flip-flop U4A is always high at the beginning of a count sequence. The low output from the $\overline{Q}$ is applied to NAND U3D and to the prescaler U2.

So far the discussion assumed an initial condition of 0's loaded into U5 and established that the divide-by-11/divide-by-10 prescaler always begins in the divide-by-11 mode. Assuming 0's as an intial condition also served to explain the function of the two flip-flops in preventing 0's from dropping the data input of U4B low. If any other number is loaded into counter U5, it simply decrements to 0, and the conditions just explained take place. Of course, the prescaler divides-by-11 for the additional states before reverting to divide-by-10.

Phase/Frequency Detector U15A. - This stage receives a fixed 10 kHz reference at its reference input, pin 3, and a divide-by-N input frequency at its variable input, pin 1. When the loop is locked, the divide-by-N frequency will also be 10 kHz, and only a slight phase difference will exist between the two inputs.

If the frequency and phase match exactly, outputs U1 and D1 remain high. If the variable input from the divide-by-N stage lags in phase, U1 goes low. If it leads in phase, V1 goes low. For an initial condition, as when the unit has first been turned on, the output states of U1 and D1 are undetermined. This results from the sequencial operation of the detector, and lasts for about 10 input pulses.

In actual practice under lock conditions, there will be output pulses from U1 and D1, but they will be extremely narrow and will show up on an oscilloscope as spikes. They result from propagation delay in the detector. For a large difference, as when the divide-by-N changes to establish a new VCO frequency, the detector responds to the change as described above, and wide pulses appear on the appropriate output.

Other considerations pertaining to the phase frequency detector should be remembered. The two inputs respond only to the negative going edge on the input signals. This means the duty cycle of the reference input and the variable input has no effect on operation. The high level to pins 1 and 3 must be greater than 1.8 volts and the low level must be less than 1.1 volts. For output pins 2 and 13, the high level must be greater than 2.5 volts, and the low level must be less than 0.4 volts.

Charge Pump Q3-Q4. - Transistors Q3 and Q4 are biased off. Thus under static conditions the output of the charge pump at the junction of R21 and R22 would rest at 0 volts.

When the VCO frequency goes low, negative pulses appear at D1 of U15A. These pulses couple through potentiometer R16 to the base of Q3 which is connected as a common emitter stage. Negative going pulses on the base of Q3 appear as positive going pulses in the collector stage. These pulses couple to integrator U22.

When the VCO frequency goes high, negative pulses appear at U1 of U15A. Inverter U16C makes positive pulses which couple through VR1 to transistor Q4. It too is connected as a common emitter stage, so negative pulses appear in the collector stage. These pulses couple to integrator U22.

Potentiometers R15 and R16 are set so their related transistors are just ready to turn-on when not being pulsed. In practice, the adjustments are performed under dynamic conditions. Voltage regulator VR1 sets up the voltage for the base of Q4 so that U16C is just able to turn the transistor on and off.

Integrator U22. - Operational amplifier U22 integrates any voltage appearing at its input. An integrator is a circuit that takes the sum of the input signal over a period of time. When a constant voltage is applied to the input of U22, a constant charge current is applied to C22, and the voltage across it increases linearly. If the input to U22 were a square wave, the output would be an inverted triangular wave.

When the VCO frequency is too low, Q3 supplies positive pulses to U22. These are integrated as a negative going voltage. When the VCO frequency is too high, Q4 supplies negative going pulses to U22. These are integrated as a positive going VCO tuning voltage which then lowers the VCO frequency.

Line Receiver U1. - These three stages increase the 1st LO VCO (A15) signal from a nominal value of 70 mV to an 800 mV peak-to-peak signal riding on a 3.5 volt dc level. Potentiometer R8 should be adjusted for the 800 mV peak-to-peak signal at pin 14 of U1C.

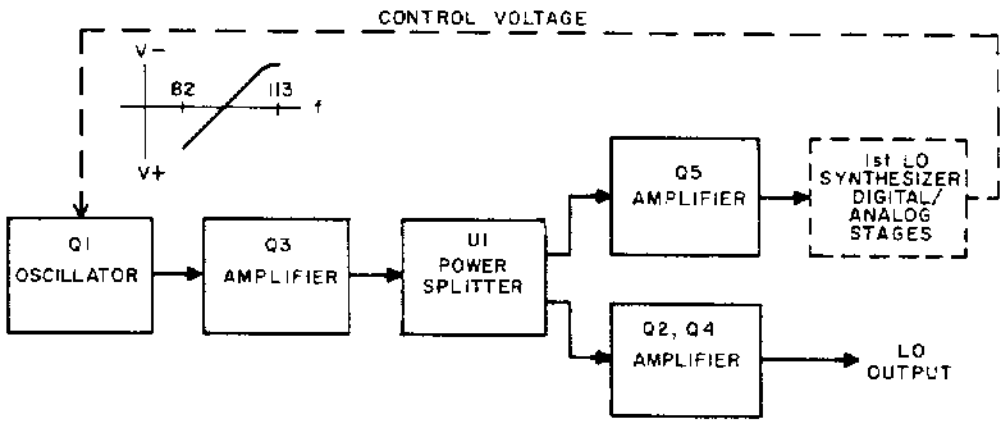


Figure 4-13. 1st LO VCO Functional Block Diagram

Type 791271 VCO Assembly A15. - Figure 4-13 is the functional block diagram for this assembly. The VCO is an integral part of the 1st LO synthesizer loop, the other portion being indicated by the dashed block supplying the control voltage. Oscillator stage Q1 receives a +10 to -10 volt control voltage from the digital/analog portion of the 1st LO synthesizer. This voltage tunes the oscillator from 83.31 MHz to 113.30 MHz in 10 kHz steps. The oscillator output routes through amplifier Q3 to power splitter U1 which supplies amplifier Q2/Q4 and amplifier Q5 with a portion of the oscillator signal. Amplifier Q5 provides the digital portion of the synthesizer with a sample of the oscillator signal. The sample is processed and, if required, a slight correction made to the control voltage. Amplifier Q2/Q4 supplies a high-level signal for the 1st mixer. For a detailed description of the VCO, refer to the next paragraph.

VCO A15 Detailed Descriptions. - Refer to Figure 7-17 for the schematic diagram of this assembly. This detailed description follows the same organization as the functional description given in the preceeding paragraph.

Control voltage from the analog stages of the synthesizer enter the assembly at pin 2. This voltage operates in the range of +10 volts to -10 volts; the corresponding frequency change of the oscillator is approximately 83.31 MHz to 113.30 MHz. The relationship between the control voltage and oscillator frequency is not exact. For example, if +10 volts corresponded to an oscillator frequency of 83.31 MHz, and if heat were applied to the oscillator portion of the VCO, there would be a tendency for a frequency change. However, this tendency would be opposed by a corresponding change in the control voltage. The net effect would be the same frequency, but a slightly different control voltage.

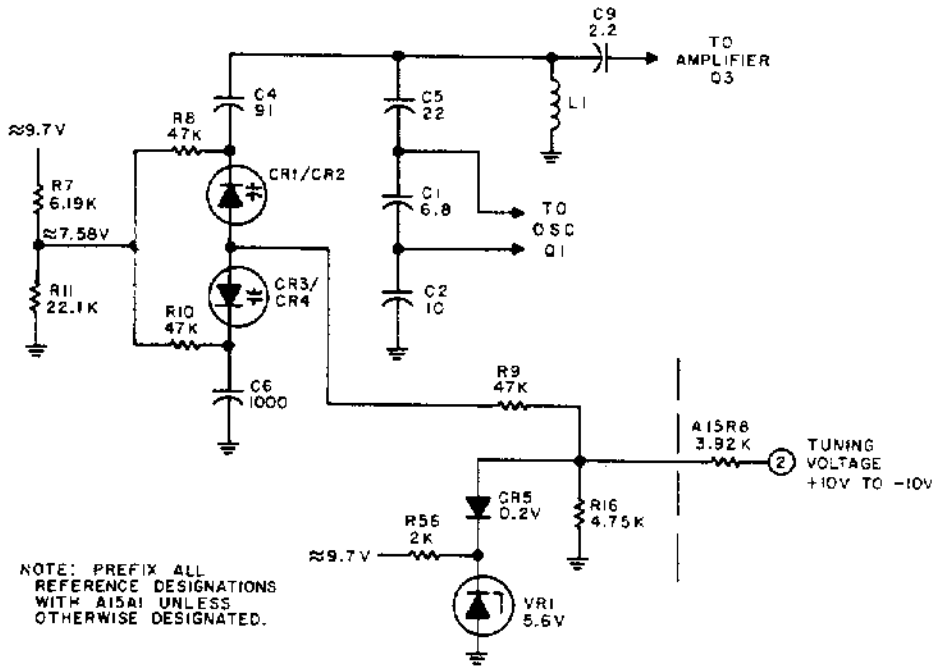


Figure 4-14. 1st LO VCO Tank Circuit Simplified Schematic

Figure 4-14 is a simplified schematic diagram of the VCO tank circuit and its control voltage input stages. Tuning voltage applied to pin 2 drives a divider made up of A15R8 and R16. The ratio of these two resistors establishes a voltage at their junction that is 0.55 of the voltage at pin 2. For example, if the voltage at pin 2 were 9 volts, the voltage at the junction of A15R8 and R16 would be 4.93 volts. On positive excursions of the control voltage, diode CR5 will conduct if the voltage at the junction of A15R8 and R16 becomes greater than 5.8 volts. This action takes place because voltage regulator diode VR1 clamps the cathode of CR5 at 5.6 volts. When the voltage on the anode exceeds about 5.8 volts, the diode is forward biased and the control voltage begins to limit. The actual effect of this is to clamp the positive voltage at R16 to +6 volts. On negative excursions, however, the diode is reversed biased at all times and no limiting is provided.

Control voltage is applied to the anodes of the balanced varactor diodes through R9. Cathode voltage for the varactor diodes is held at approximately 7.6 volts by the resistive divider R7/R11. Because there is neglible current flow through the reverse biased diodes the voltage drop across R8, R9, and R10 is also negligible. These resistors provide isolation for the oscillator signal.

Coil L1 is the tank circuit inductor. In parallel with the inductor are the capacitive elements. Capacitors C5, C1, and C2 make up one portion of the capacitance. Oscillator FET Q1 receives its ac signal from these elements. Capacitors C4, CR1/CR2, and CR3/CR4 make up the other portion of the tank capitance. The varactors in this leg provide the tuning for the tank. Capacitor C6 provides an ac ground for this leg; however, it is not a part of the tuning

for the tank circuit. The large value has a negligible effect for the frequencies of operation.

Varactor cathodes are held at 7.6 volts. Voltage on the anodes may vary from about +5.5 volts to -5.5 volts. The net reverse-voltage across the varactors, then, can be from 2.1 volts to 13.1 volts. With 13.1 volts reverse bias on the varactors, oscillator frequency will be approximately 113.30 MHz. Conversely, with minimum reverse bias applied to the varactors, maximum capacitance is developed, and frequency will be at a minimum, 83.31 MHz.

Oscillator transistor Q1, which is shown in Figure 7-17, operates in the common-drain mode and is a low-level clapp circuit. Regeneration to sustain oscillation developes across R2, and couples to the gate through C1. The gate and the source are in-phase for this N channel FET; therefore, each increase in signal across the source resistor provides the gate with a signal that further increases the signal on the source resistor.

Output from the tank circuit couples through C9 and a 4 dB isolation pad to the base of Q3. The collector stage of this transistor contains a coupling transformer for impedance matching to the power splitter. The 3 dB pad between the transformer and the power splitter improve the input impedance to the splitter.

There are two outputs from the splitter. Signal from pin 5 of U1 is a part of the 1st LO synthesizer loop. Approximately 12 dB of attenuation results from the pad connected to E2. Level adjustment can be performed by changing the value of R41. Following the pad, a high-pass filter prevents signal from the 1st LO synthesizer digital/analog section from coupling into either the 1st LO oscillator stage or the LO output path to the converter. From the filter, signals couple to the base of Q5, are amplified, and then couple from T2 to the output at pin 20. Isolation and impedance matching for the output is provided by the 6 dB pad, R44, R47, and R48.

Returning to the power splitter, signals from U1 pin 6 are routed to the base of Q2. From Q2 they are amplified, coupled to T3, then to a 3-dB isolation pad. From there, the signals are amplified by Q4 then coupled from T4 to the LO output, A1J1. L4 and R35 form a feedback network for Q4.

Both the +15 and -15 volt power lines in the assembly are filtered to minimize external noise, especially 60 Hertz power line components. Heavy filtering in the base circuit of Q1 provides 40 dB isolation at 60 Hertz. A 10.3 volt base-bias establishes an emitter voltage of about 9.7 V dc. Transistor Q2 provides only amplifier stages with current, so it is filtered with a single capacitor, C5.

4.4.4 2ND LO SYNTHESIZER. - The 2nd LO tunes from 72.100 00x to 72.109 99 x MHz in steps of 10 Hertz. Figure 4-15 shows a functional drawing of the 2nd LO. In essence, two signals are generated (one fixed, one variable) to create a third signal, which is the actual 2nd LO output frequency.

The variable portion of the 2nd LO appears at the top of the figure. The VCO provides a signal to the divide-by-10/divide-by-11 stage which works in conjunction with the other divide-by-N stages to supply a reference signal to the phase detector. This signal is compared to a 10 kHz reference signal.

The phase detector then produces positive and negative pulses related to the difference between the two, which the integrator converts to a dc voltage. This voltage controls the VCO frequency, either maintaining lock, or driving the VCO frequency in the correct direction to re-establish lock.

Returning to the divider stages, the look-ahead feature completes the last three counts of the sequence thus allowing the dividers to be reset in preparation for the new count sequence.

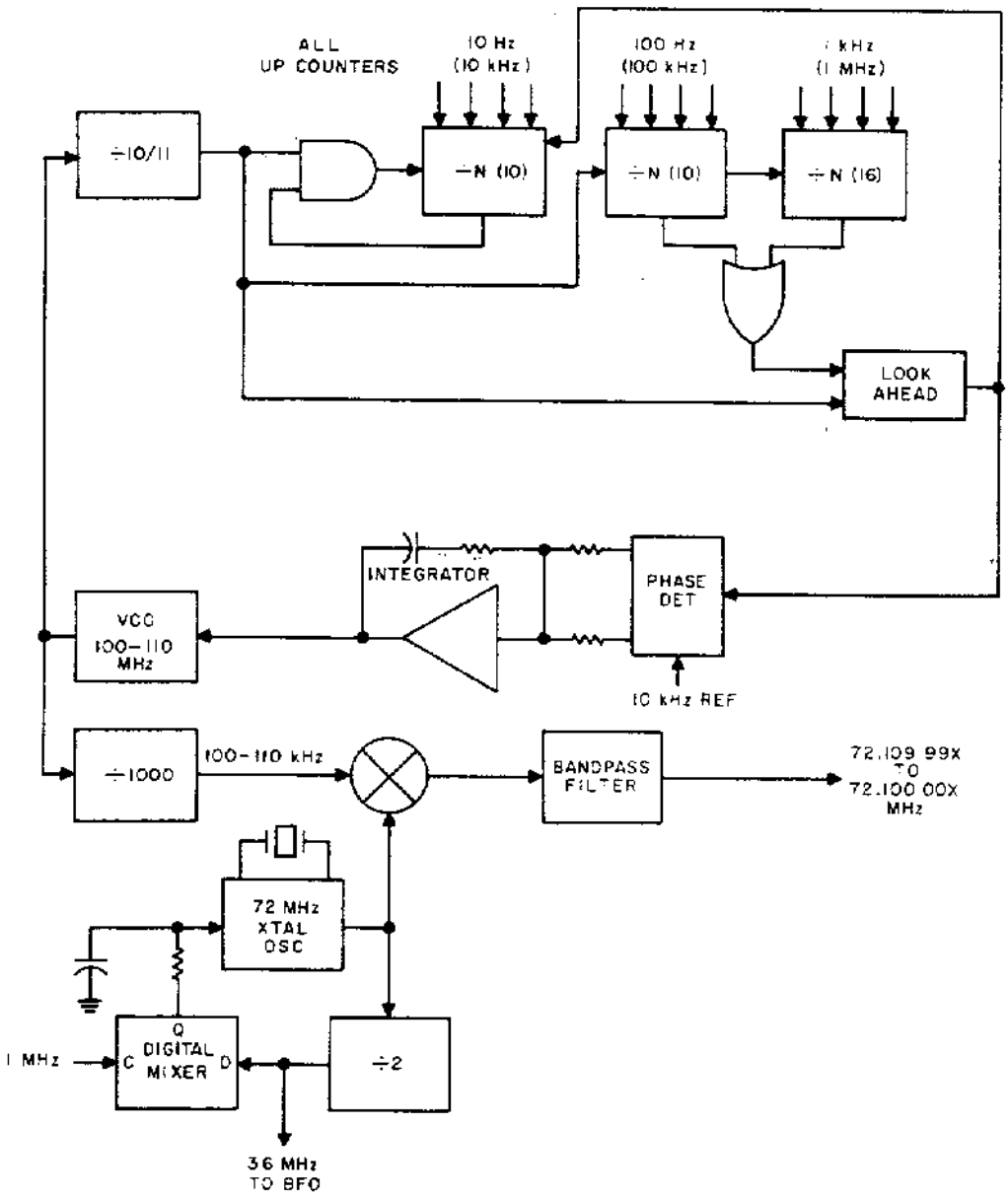


Figure 4-15. 2nd LO Functional Diagram

Output from the VCO routes through a divide-by-1 000 stage to a mixer. This signal, in the range of 100.00x kHz to 109.99x kHz, sums with the fixed 72 MHz signal to produce the 2nd LO output frequency range of 72.100 00x to 72.109 99x MHz.

Digital mixing maintains frequency of the 72 MHz stages of the 2nd LO. In brief, the technique involves sampling the 72 MHz oscillator frequency, at the 1 MHz reference frequency rate. The Q output is integrated and the resulting dc voltage controls the oscillator frequency. For a more detailed explanation of the 2nd LO continue to the following paragraphs.

Divide-By-N Integrated Circuit Data. - Integrated circuits U11, U15, and U17 are BCD up-counters (0 through 9). U20 is a binary up-counter (0 through 15). Otherwise these four counters are the same. Only characteristics applicable to their use in the 2nd LO divide-by-N stages will be described.

The counters increment on the low-to-high transition of the clock, but only if the parallel enable ($\overline{PE}$), count enable parallel (CEP), and count enable trickle (CET) all are high. Terminal count output is high when a counter is at terminal count (state 9 for U11, U15, and U16; state 15 for U20) and when CET also is high. Delay from clock pulse to terminal count output and Q outputs is about 25 ns. Therefore, if the terminal count output of one counter enables the CET input of another counter, and both counters receive the same clock pulse, the second counter cannot increment with the first counter. But, the next clock pulse will increment the second counter before the terminal count from the first counter is removed.

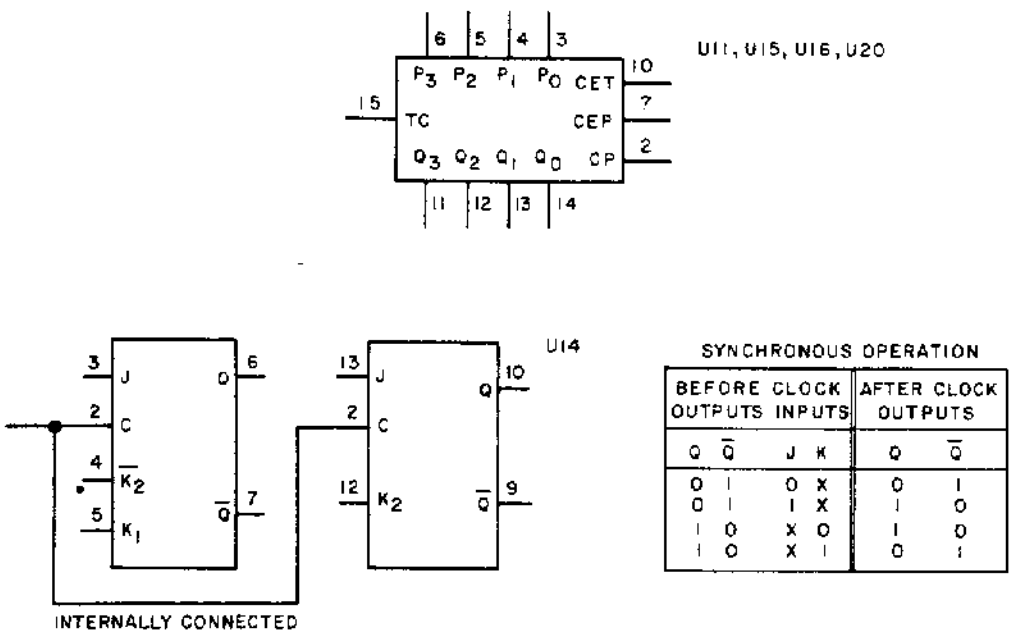


Figure 4-16. 2nd LO Divide-By-N Integrated Circuits

When a counter is preset, by application of a low to the $\overline{PE}$ input, the Q outputs do not change until the first low-to-high clock transition following the low state to $\overline{PE}$. This is an important consideration in the look ahead feature involving flip-flops U14A and U14B. Also, CEP and CET inputs float high unless pulled low.

When $\overline{PE}$ is low, the counter can be loaded with any number in its sequence by applying the desired parallel data at inputs P0, P1, P2, and P3. For example, if a counter is loaded with a 4 (P2 is high and the other P inputs low), the first clock pulse transferes the 4 from the P inputs to the Q outputs. Successive pulses then increment the counter through normal sequence (5, 6, 7 etc.,) to its terminal count (9 or 15) and then to zero. The counter continues in its normal sequence (1, 2, 3, 4, 5, 6, etc.,) and does not reset to the 5 state. Only when the $\overline{PE}$ input goes low does the counter load the states present at the parallel inputs.

The divide-by-10/divide-by-11 prescaler (U11) is an ECL device capable of operating at the 2nd LO upper frequency limit of 110 MHz. Its unique characteristic is the ability to switch between the two divide ratios so that no clock pulses are lost. Clock pulses enter the prescaler on pins 1 and 16. Output is taken from the Q and $\overline{Q}$ outputs, pins 8 and 9. A low at $\overline{PE}$ pin 2 establishes a divide-by-11 action. Conversely, a high there causes the prescaler to divide-by-10.

This dual modulo action results from the following sequence within the presecaler. Output Q4 is low for 5 incoming clock pulses and high for the subsequent 5 or 6 incoming clock pulses. The decision between the two modes results from the state of input $\overline{PE}$. If this input is low 5.4 ns before the rising edge of Q4, then Q4 will stay high for 6 incoming clock pulses (divide-by 11). If PE is high before the rising edge of Q the output will stay high for 5 clock pulses (divide-by-10).

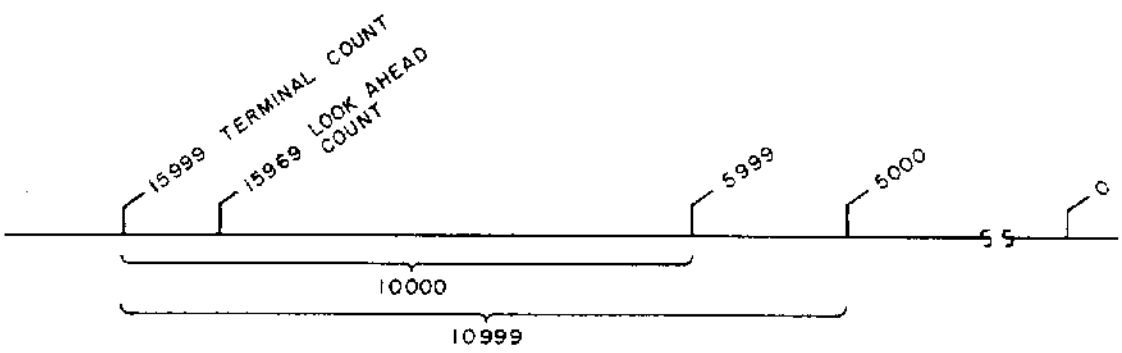


Figure 4-17. 2nd LO Divide-By-N Range

Flip-flops U14A and U14B. - Both of these are master/slave JK types. Data is accepted by the master when the clock is in the low state. Transfer from the master to the slave occurs on the low-to-high transition of the clock. When the clock is high, the J and K inputs are inhibited. The truth table defines the outputs after a low-to-high transition the clock pulse.

Divide-by-N Stages. - This portion of the 2nd LO receives the VCO output at pins 1 and 16 of U6, and provides a divided output from pin 15 of U20 for use by the phase comparator. When the loop is locked, the output will always be 10 kHz. The input from the VCO, however, can be in the range of 100.000 000 MHz to 109.990 000 MHz. To divide 100.00x MHz down to 10 kHz requires a divide ratio of 10 000. To divide 109.99x MHz down to 10 kHz requires a divide ratio of 10 999. For any VCO frequency between 100.00x MHz and 109.99x MHz, then, the divide ratio must fall between 10 000 and 10 999. From this it is evident that only the three least significant digits must be manipulated to give the total range of required divide ratios. This is, in fact, what is done. Counters U16, U15, and U11 are each programmable from zero through nine. Counter U20 is a hexadecimal (0 through 15) device which is hard wired for a five. In effect then, it is a count by ten stage.

An example will help clarify the divide ratios. If U20 were not hard wired to a five, and if U16, U15, and U11 were loaded with zeros, then a maximum count of 15 999 would be available. This is because the counters start at 0000 and increment up to 15 999. This condition appears in row A of Table 4-5. Row B shows U20 loaded with a five, which is its actual hard wired condition. The other counters remain loaded with zeros. The resulting maximum count is 10 999. With U16, U15, and U11 loaded with nines (and U20 still hard wired for 5) the conditions of row C result. The count would then be 10 000. Loading U16, U15, and U11 with numbers between 000 and 999 will give the total range required. With this overall operation complete, a more detailed discussion may be undertaken.

Table 4-5. 2nd LO Counter Range Restriction

A	15	9	9	9
	0 (U20)	0 (U16)	0 (U15)	0 (U11)
	15	9	9	9
B	15	9	9	9
	5 (U20)	0 (U16)	0 (U15)	0 (U11)
	10	9	9	9
C	15	9	9	9
	5 (U20)	9 (U16)	9 (U15)	9 (U11)
	10	0	0	0

Count Sequence of U15, U16, and U20. - For these counters to increment, CEP, CET, and $\overline{PE}$ must all be high. The CEP and CET inputs float high if not connected. Also, the terminal count output lags the initiating clock pulse about 15 ns because of propagation delay. Thus, when a terminal count enables the next most significant digit(s), it is the following clock pulse that increments it (them). Propagation delay also prevents removal of the enabling terminal count before the clock pulse increments the counter(s).

For example, when U15 receives a clock pulse incrementing it from an 8 to its terminal count of 9, the terminal count output does not go high until 15 ns after the leading edge of the clock pulse. Because the clock pulse (CP) input of

these counters respond only to the positive-going edge of the pulse, U16 is clocked before being enabled, and it cannot increment. On the positive going edge of the next clock, however, both U15 and U16 increment. Propagation delay prevents the terminal count being removed from U15, and U16 increments.

Notice that for U20 to increment, both U15 and U16 must be at state 9. Their terminal count outputs then enable the CEP and CET inputs of U20. The next clock pulse increments all three counters before any terminal count output can go low.

When U20 increments to 15, its terminal count output goes high. This high is applied to flip-flop U14A as a part of the look-ahead enabling.

For the terminal count output of U20 to go high when it increments to state 15, its CET input must also be high. Thus, the terminal count output from U20 does not enable flip-flop U14A until counter U16 increments to 9 and provides U20 with a high on its CET input.

Terminal count is 15 999. Look ahead is three counts before that, or 15 969. (The 9 in the least significant digit position is determined near the beginning of the count sequence.) With U20 and U16 at states 15 and 9, respectively, only U15 need increment to the look-ahead number. Thus, U15 is always the last counter to increment to the look-ahead number. When it reaches 6, NAND U7C receives highs on both inputs, and its output is driven low. This initiates the 3-count sequence of the flip-flops during which the counters are reset and a pulse provided to the phase comparator.

Look Ahead Flip-Flop U14. - Look ahead is initiated when the most significant digit, U20, reaches state 9 and 100 s Hertz digit U15 reaches a state 6. The terminal count from U20 applies a high to K1 of U14A. The 6 on U15 applies two highs to the input of NAND U7C. The resulting low from the NAND takes the $\overline{K2}$ input of flip-flop U14A low causing it to change state.

TRUTH TABLE

BEFORE CLOCK OUTPUTS		INPUTS		AFTER CLOCK OUTPUTS	
Q	$\overline{Q}$	J	K	Q	$\overline{Q}$
0	1	0	X	0	1
0	1	1	X	1	0
1	0	X	0	1	0
1	0	X	1	0	1

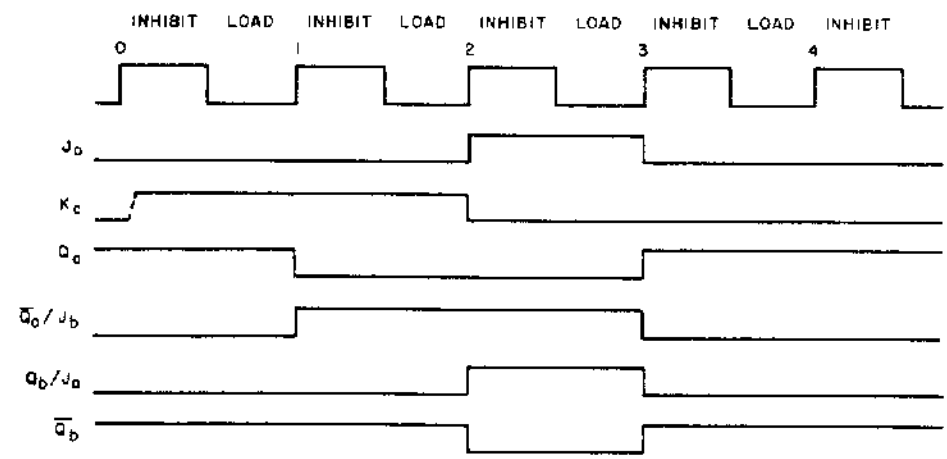


Figure 4-18. 2nd LO, Flip-Flop Terminal Count Completion

Figure 4-18 gives the timing diagram and truth table for look ahead flip-flop U14. The clock pulse rising edge indicated by the 0 increments U15 to state 6--which initiates the look ahead. On the timing diagram, Ka represents the composite of K1 and $\overline{K2}$. That is, K1 must be high and $\overline{K2}$ must be low for the Ka input to represent a high state. The dashed leading edge of Ka indicates propagation delay, but is on no consequence because flip-flops a and b load during the low state of the clock, before the rising edge of clock pulse 1. At the rising edge of clock pulse 1, Qa goes low, and $\overline{Q}$a/Jb goes high. The Q outputs of flip-flop U14B do not change state because input Jb was low during the load period of the clock before rising edge 1.

Counters U15, U16, and U20 receive the low from Qa on their $\overline{PE}$ inputs. However, they do not change the state of their outputs until being clocked after their $\overline{PE}$ inputs go low. For this reason, Ka stays high until clock pulse 2 is applied to the three counters. With Ka still high during the load period (clock low) just before clock pulse 2, outputs Qa and $\overline{Q}$a maintain their states.

Clock pulse 2 also changes the state of U14B. With Jb high during the load period (clock low) prior to clock pulse 2, outputs Qb and $\overline{Q}$b change state on the rising edge. The low from Qb is applied to the $\overline{PE}$ input of counter U11. On the next clock pulse, this counter will change state and set the prescaler to divide-by-11.

Clock pulse 3 causes $\overline{Q}$a to go high and Qa to go low. It also changes the state of $\overline{Q}$b and Qb so they become low and high, respectively. Refering to the truth table and the states of the inputs of U14A and U14B during the load period prior to clock pulse 3 will confirm these new states. Notice that the states of all flip-flop terminals are back to their conditions prior to clock pulse 0.

Phase/Frequency Detector U29A; Charge Pump U29B; Lag/Lead Active Filter Q8/U29C. - These stages are functionally identical to BFO stages described on page 4-26. Differences will be described here. Otherwise, refer to the BFO descriptions.

The 2nd LO uses a 10 kHz reference frequency for the phase/frequency detector. NAND U7D gives a high output if either input goes low, an indication of unlock. Filter R1-C1 removes the spikes always present with a lock condition, thus preventing a false indication of unlock.

Divide-By-1 000 Stages. - Output from VCO U4 must be divided-by 1 000 to give the 100.00x to 109.99x kHz required for mixing to produce the 2nd LO output. Flip-flop U3 operates at the same ECL levels as the VCO, and divides the signal by 4. ECL-to-TTL level conversion by Q12 then provides a clock for U5. A divide-by-250 action in stages U5, U10, and U9 combine with the previous divide-by-4 to give the required divide-by-1 000. The 100.00x to 109.99x kHz output from U9 supplies mixer U8 with a variable frequency signal to produce the 2nd LO tuning range.

72 MHz Oscillator, and Mixing. - Figure 4-19 shows the mixing of the divided-down 109.99x to 100.00x MHz synthesized signal with the 72 MHz signal.

This produces the actual 2nd LO frequency range of 72.109 99x to 72.100 00x MHz. Refer to Figure 7-21 for the schematic diagram of these stages.

Differential amplifier U2A is connected as an oscillator stage. Pin 4 is maintained at RF ground by C8 and C9. Parallel resonance across the input of the differential amplifier is provided by C7, C10, and L3. Positive feedback through series resonance circuit C11, CR7, Y1, and L2 sustains oscillation. Varactor CR7 keeps the oscillator at exactly 72 MHz by pulling crystal Y1 to maintain frequency.

Phase comparison in U1A provides the tuning voltage for the varactor diode. Pin 6 of U1A receives a 1 MHz reference signal from the time-base dividers. Input D1 receives a 36 MHz signal which was divided down from the 72 MHz oscillator signal.

The outputs from the flip-flop turn Q3 on and off, which charges and discharges C5. Gain loop bandwidth of the 72 MHz oscillator is primarily determined by C5 and R11. Isolation between the RF and dc stages is provided by R19. Capacitor C4 provides roll off at about 1 MHz.

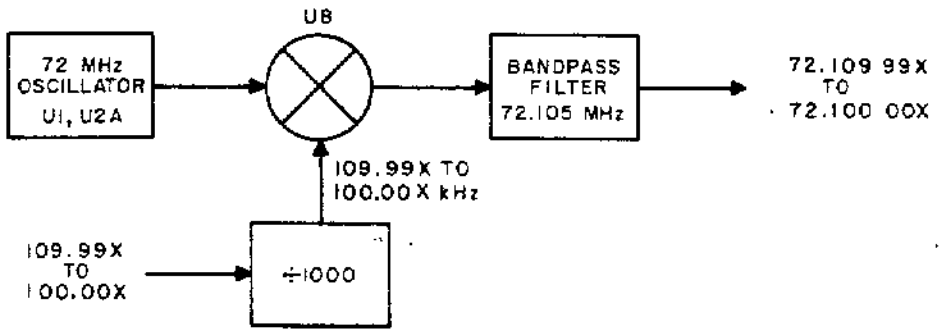


Figure 4-19. 2nd LO VCO Conversion To 72.105 (±) MHz

Buffer U2B drives the mixer through crystal Y2, which gives a high degree of filtering to the 72 MHz signal. In mixer U8, the 72 MHz combines with the 109.99x to 100.00x kHz signal from the dividers. Differential amplifier U2C drives the filter stage, which rejects the difference output from the mixer. The sum signals of 72.109 99x MHz to 72.100 00x MHz, then, appear at the output of the board, pin A5.

Filter FL1 is a 4-pole type having a bandwidth of 20 kHz. Coils L9 and L10 should be adjusted for a response flat to within about 0.5 dB across the range of the 2nd LO. Output levels from the board should be at least 50 mV.

Counters U3A and U3B use emitter coupled logic levels, so transistor Q12 converts the signal to TTL levels to drive U5.

4.4.5 3RD LO SYNTHESIZER. - This LO operates on a fixed frequency of 11.155 000 MHz ± 1 Hz. It is a part of the type 791109 1st LO/3rd LO/Time

Base Circuit board. Location of components are given in Figure 6-29. Refer to Figure 7-20 for the schematic diagram. Pins AM, BB, and AX at the upper right of the schematic diagram locate the 3rd LO components.

Phaselock Loop U25. - Figure 4-20 shows a simplified schematic diagram of the 3rd LO. Included in the drawing are functional blocks for phaselock loop stages of U25. Output frequency results from the parallel combination of C29 and C30. Crystal Y1 prevents the loop from locking to an incorrect 5 kHz harmonic and does not control frequency.

The 11.155 000 MHz output from the VCO routes through A3 to pins 3 and 4 of U25. The signal from pin 3 enters the data input of the mixer where it combines with a 50 kHz reference applied to the clock input. The result is a 5 kHz output at Q and $\overline{Q}$. An explanation of the mixer operation follows the information about U25. The 5 kHz complementary signals applied to pins 2 and 15 are compared with a 5 kHz reference signal applied to pin 12. The phase comparator developes correction voltage which stage A1 integrates. Associated with A1 are filter components C36-R49 and C35.

They determine loop response time, capture range, and bandwidth. Control voltage from A1 routes through A2 before being applied to the VCO. Pin 9 of the IC is a convenient monitoring point for this voltage.

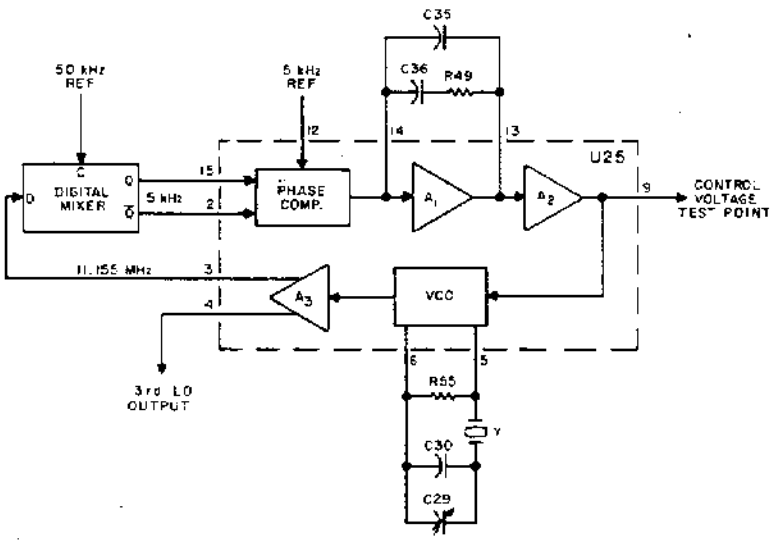


Figure 4-20. 3rd LO Simplifed Schematic

Refer to Figure 7-20, the schematic diagram, for the remainder of the 3rd LO circuit description. Transistor Q5 provides a clean, TTL level, square wave for the data input of U18B. To match the Q and $\overline{Q}$ outputs to the phaselock IC requires level translation. Resistors R42, R46 and R43, R47 do this. Pin 1 of U25 is a reference source for the translation. The 3rd LO output is taken from pin 4. Level for this 11.155 000 MHz signal at the circuit board output, pin AX, should be at least 70 mV.

FIGURE 4-21 WJ-8888

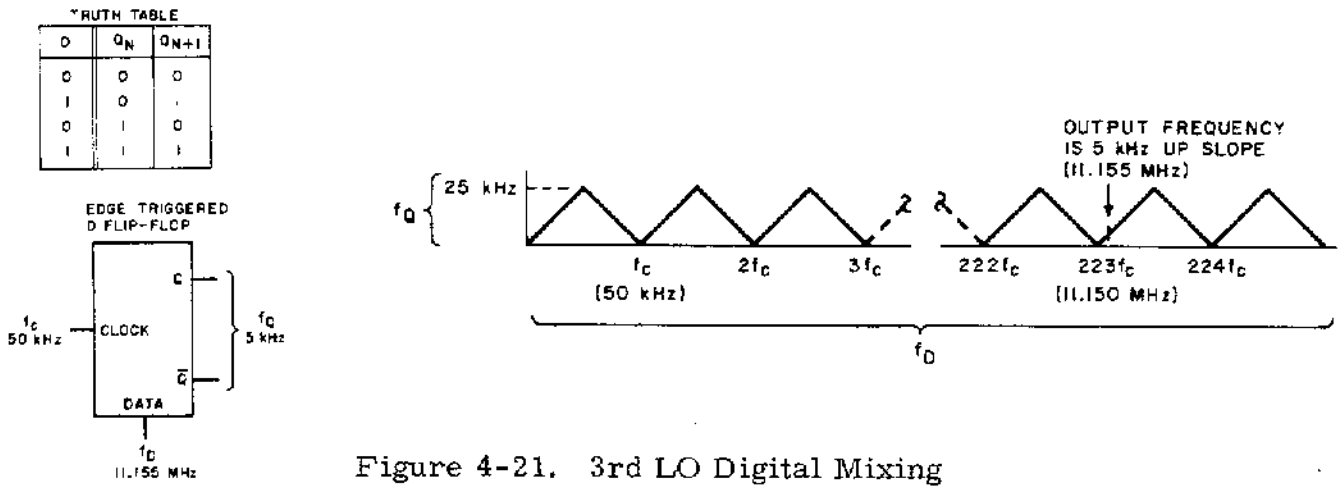


Figure 4-21. 3rd LO Digital Mixing

Digital Mixing. - An edge triggered D flip-flop can be used to mix two signals, thereby creating a third signal at the Q outputs. Figure 4-21 shows a D flip-flop and its truth table for the Q output. If the data input is a logic 1 when the clock makes its transition, the Q output goes to a 1 and remains there for the full clock period. If it is a 1 from the previous period, it remains a 1. The inverse holds true for logic 0 inputs.

In effect then, the clock is sampling the data input, and transfering the information to the Q output. Several characteristics of D-type mixing appear in the drawing. If the flip-flop were clocked at a 50 kHz rate, and if a frequency counter were connected to the Q output, the indication would be 0. Then if a signal generator were connected to the data input and the frequency slowly increased from 0 to 50 kHz, the output frequency would increase to a maximum of 25 kHz and then decrease to a null. If the signal generator were tuned from 50 kHz to 100 kHz, the frequency counter would give an indication of 25 kHz and then decrease to a null again when the signal generator frequency reached 100 kHz.

This would show that the output frequency from a D-type mixer cannot exceed one-half of the sampling frequency. Furthermore, the points where the frequency at the Q output nulls occurs at integral multiples of the sampling frequency.

For the example based on the 3rd LO, the 223 multiple of the 50 kHz sampling frequency is 11.150 MHz. When 11.155 MHz is supplied to the data input, an output frequency of 5 kHz is established at the Q outputs.

4.4.6 BFO SYNTHESIZER. - This synthesizer produces a signal which can be tuned in the range of 8476 to 10 524 MHz. This is mixed with a 36 MHz signal then divided-by-100 to produce the 455 kHz BFO frequency. It is a part of the type 791117 2nd LO/BFO circuit board. Figure 7-21 is the schematic diagram. Location of components appear in Figure 6-30.

A functional diagram, devoted primarily to the divide-by-N stages, appears in Figure 4-22. Output from the VCO gets divided in the four down-counters. The resulting output pulses are compared with a 1 kHz reference in the phase detector. If the two signals are not the same frequency, the phase detector produces either positive or negative output pulses, depending on the direction of the error. Integrating these pulses shifts the dc voltage which then drives the VCO in the proper direction to re-establish the desired frequency.

FIGURE 4-22

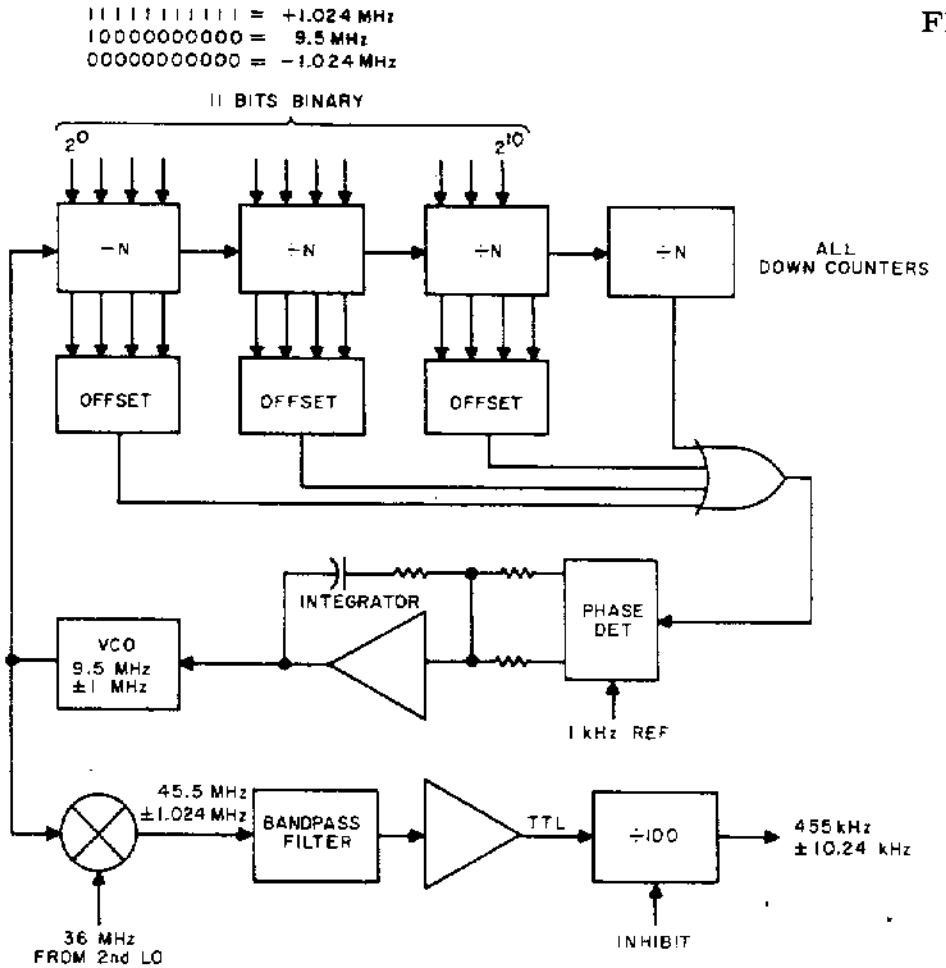


Figure 4-22. BFO Functional Diagram

Output from the VCO combines with a 36 MHz signal derived from the 2nd LO. When the VCO frequency is locked at 9.5 MHz, the center of its range, output from the mixer is 45.5 MHz. This routes through a bandpass filter to amplifier stages which provides TTL levels to the divide-by-100 stages. Their 455 kHz output receives an on/off command at the inhibit input.

Divide-By-N Integrated Circuit Data. - Counter U17, U21, U25, and U30 are TTL down counters that can be programmed for any initial state, 0 through 15. These counters decrement on the positive going edge of the clock pulse. The buss output goes high in the 0 state and remains there until the leading edge of the clock pulse produces the transition to 15. A low state applied to the $\overline{PE}$ input enables P0 thru P3. But the data does not transfer to the Q outputs until the positive-going edge of the next clock pulse. Also, the clock pulse transferring the data to the Q outputs does not decrement the counter. The P0 through P3 inputs are independent of the logic level of the clock. Entering a number in them causes the counter to begin its count at that number. But until $\overline{PE}$ goes low again, the counter decrements through its normal sequence and does not reset to the number applied to the P inputs.

FIGURE 4-23
FIGURE 4-24

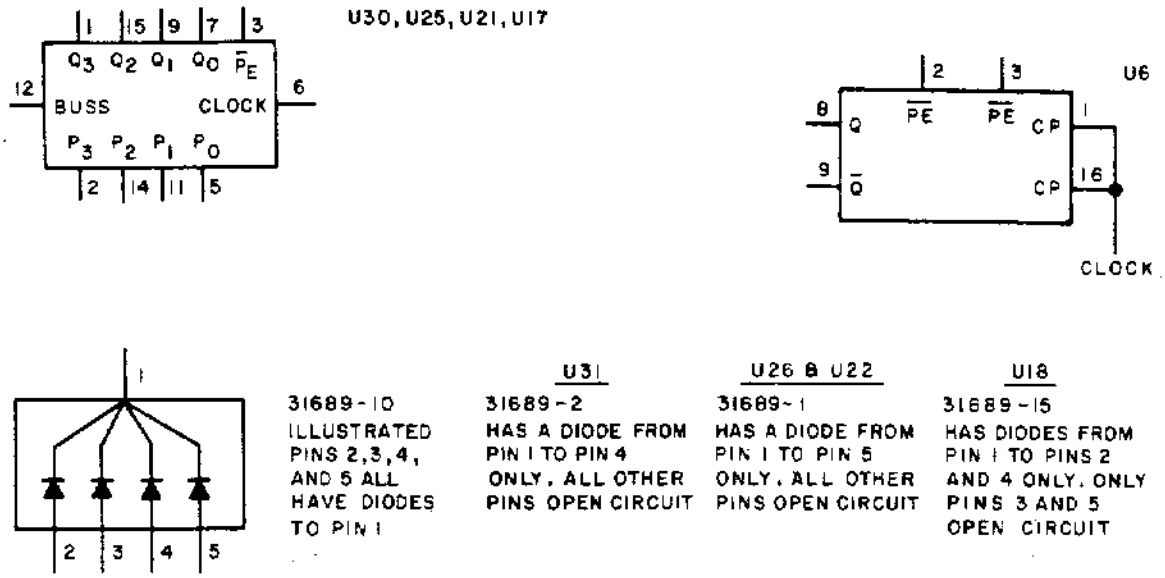


Figure 4-23. BFO Divide-By-N Integrated Circuits

Divide-by-N Stages. - These stages must give a 1 kHz output for all input signals in the range of 8.476 to 10.524 MHz. To do this, they must provide a divide ratio of 8 476 to 10 524 thereby converting all possible input frequencies to 1 kHz.

The basic divide capability of these stages is 65 536. That is, U17, U21, U25, and U30 each provide a divide-by-16 action. (16 x 16 x 16 x 16 equals 65 536). For this divide ratio the input frequency would have to be 65.536 MHz to get an output frequency of 1 kHz. Because the VCO must operate in the range of 8.5 MHz to 10.5 MHz, the basic counter stages must be modified.

Preventing them from counting down the entire 65 536 counts is one method. If the offsets shown connected to the counters stopped the count at 57 061 then terminal count would occur after 8475 increments (65 536 minus 8475 equals 57 061). With the offsets in the circuit, the VCO would maintain a frequency of 8.475 MHz. Because one clock pulse is used to reset the count chain, the effective offset is one count more--8476. This number will be used for the remainder of the BFO circuit descriptions. It is 24 kHz below our desired minimum frequency of 8.5 MHz, but other circuit actions establish the required range, as the next paragraph will explain.

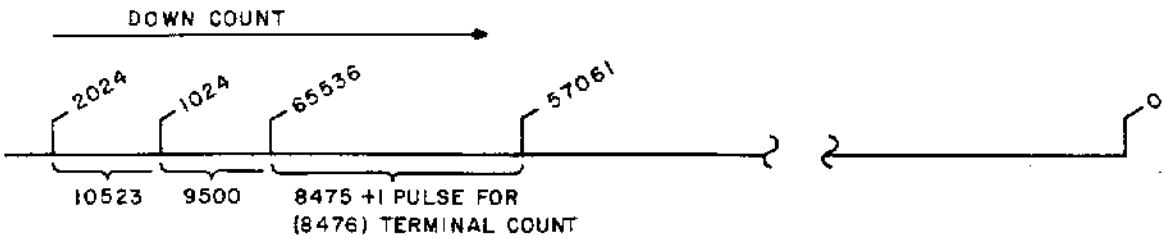


Figure 4-24. BFO Divide-By-N Range

With the counters now restricted to a divide ratio of 8476 by the offsets, a method is needed to increase the divide ratio so that 10.5 MHz can be divided down to 1 kHz. To increase the divide ratio requires additional counts. To gain these, the four counters start their sequence not from 65 536, but instead from some state before that. That is, normally each one would start from 0 and decrement to 15, 14, 13, etc., until each counters was at its terminal count. If a counter is loaded with any number other than 0, it must first decrement from that number to 0. Then it continues through its normal sequence decrementing to 15, 14, 13, etc., until each counter has decremented to its terminal count, when the sequence would begin again. If all the parallel inputs were given a high state, the maximum count increase would exist.

The decimal equivalent of adding the 2^0 through the 2^{10} binary inputs is 2047. Table 4-6 gives the decimal equivalent for the binary inputs. If 2047 is added to the basic count capability of 8476, a total of 10 523 counts is available. By changing the binary data to the parallel inputs, any number of counts in the range of 8476 to 10 523 is available. This would correspond to VCO frequencies of 8.476 to 10 523 MHz, which exceeds the required range of 8.5 to 10.5 MHz.

To summarize then, adding the binary equivalent of 24 into the parallel inputs increases the count from 8476 to 8500. This is the number of counts required to divide the 8.5 MHz VCO signal down to 1 kHz. If the binary equivalent of 1024 is loaded into the parallel inputs, a count of 9500 exists (8476 plus 1024 equals 9500). A 9.5 MHz input to the dividers gives a 1 kHz output for use by the phase comparator. Loading the binary equivalent of 2024 into the parallel inputs, establishes a count of 10 500.

Table 4-6. BFO Binary/Decimal Equivalents

$2^{16} = 65\ 536$	$2^{12} = 4\ 096$	$2^8 = 256$	$2^4 = 16$	$2^0 = 1$
$2^{15} = 32\ 768$	$2^{11} = 2\ 048$	$2^7 = 128$	$2^3 = 8$	
$2^{14} = 16\ 384$	$2^{10} = 1\ 024$	$2^6 = 64$	$2^2 = 4$	
$2^{13} = 8\ 192$	$2^9 = 512$	$2^5 = 32$	$2^1 = 2$	

The VCO frequency established by the counters is mixed with a 36 MHz signal, and the sum output is divided by a hundred to give a BFO output in the range of 445 to 465 kHz. For example, 9.5 MHz plus 36 MHz equals 45.5 MHz. Then, 45.5 MHz divided by 100 equals 455 kHz.

An example will help explain how the counters sequence. Assume the counters are loaded on their parallel inputs for a down count of 9500. This gives a VCO frequency of 9.5 MHz, which corresponds to a BFO frequency of 455 kHz.

The binary input for a down count of 9500 exists when the 2^{10} parallel input is high and all others are low.

The first clock pulse of the new sequence decrements U17 from 0 to 15. Its Q3 output goes 0 to 1. This provides a positive-going edge to the clock input of U21, so it too decrements. The Q3 output of U21 also provides a clock pulse to U25, which decrements from state 4 to state 3. Because the Q3 outputs of these counters only go low-to-high on a 0 to 15 transition, U25 does not clock U30.

After the first clock pulse, 15 succeeding pulses would decrement U13 to a 0 state again. No other counter would have been decremented. When the next clock pulse decrements U17 from 0 to 15, another rising edge clocks U21 and it decrements from 15 to 14.

This process continues until U30 gets decremented to state 13. That is, to the first state where a low instead of a high appears on the Q1 output. A diode in module U31 connects the Q1 output to the base input of Q9. As long as a high state appears on the Q1 output of U31, the base of Q9 is held high.

After U30 decrements to 13, U4 decrements to state 14. Its Q0 output connects to the base circuit of transistor Q9. So with a state 14, a low is provided to the base.

Counter U21 connects to the base line of Q9 at the Q0 output. It makes its final decrement to a state 14, which gives a low at Q0.

After U30, U25, and U21 are all at there offset states, only U17 must decrement to its offset state. For U17, this is a 6. When a state 6 is reached, the last high holding the base of Q9 high disappears.

This occurs when the leading edge of the last pulse in the count cycle clocks U17. Output pin 1 of each of the preset modules then are at a low state. This turns Q9 off and allows the collector to go high. NAND gate U33A has high states on both pin 1 and pin 2 at this time. Output pin 3 of the NAND gate drops low, loads the four counters, and provides a clock pulse to pin 3 of phase/frequency detector U23A. (Negative transitions control U23.) One clock pulse is lost while the counters are being loaded. It is this lost pulse that is considered a part of the fixed count (8475 plus 1 equals 8476).

Phase/Frequency Detector U23A. - This stage receives a fixed 1 kHz at its reference input, pin 1, and a divide-by-N input signal at its variable input, pin 3. When the loop is locked, the divide-by-N signal will also be 1 kHz, and only a slight phase difference will exist between the two inputs.

If the frequency and phase match exactly, outputs U1 and D1 remain high. If the variable input from the divide-by-N stage lags in phase, U1 goes low. If that input leads in phase, V1 goes low. For an initial condition, as when the unit has first been turned on, the output states of U1 and D1 are undetermined. This results from the sequenctial operation of the detector and lasts for about 10 input states.

In actual practice under lock conditions, there will be output pulses from U1 and D1, but they will be extremely narrow and will show up on an oscilloscope as spikes. They result from propagation delay in the detector. For a large difference between the two input frequencies, as when the count changes to establish a new

BFO frequency, the appropriate outputs respond to the change as described above, and wide pulses appear on the proper output.

Other considerations pertaining to the phase/frequency detector should be remembered. The two inputs respond only to the negative going edge on the input signals. This means duty cycle of the reference input and the variable input has no effect on operation. The high level to pins 1 and 3 must be greater than 1.8 volts and the low level must be less than 1.1 volts. For output pins 2 and 13, the high level must be greater than 2.5 volts, and the low level must be less than 0.4 volts.

Charge Pump U23B. - This stage receives the phase detector outputs and converts them to fixed amplitude positive and negative going levels. Input to pin 11 (PD) appears as an inverted output at pin 10 (DF). An input to pin 4 (PU) appears at output pin 5 (UF) in the same state as it was received. For both outputs, the high states are leveled at 2.25 volts. The input must be greater than 2.4 volts.

Lag Lead Active Filter Q10 and U23C. - In essence, this stage is an integrator. However, basic loop characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by this filter. Positive and negative going pulses from charge pump U23B provide the input, and a dc voltage from pin 8 of U23C provides the output. This BFO tuning voltage controls the frequency of the voltage controlled oscillator stage.

Buffer Q10 provides a high input impedance for the preceeding stage. Positive and negative going pulses at the gate are developed across the source potentiometer and applied to the inverting amplifier, U29C. This inverted output couples back to the gate of Q10, thereby providing the integrated action and other circuit characteristics. Potentiometer R66, when properly adjusted, establishes zero volts for V_{GS} of Q10.

Voltage Controlled Oscillator U27. - VCO U27 is an emitter-coupled oscillator requiring an external tank circuit for operation. This tank circuit consists of L19, C42, and CR12. Varactor diode CR12 receives control voltage from the active filter. When the loop is locked, control voltage maintains the VCO in phase with the reference frequency. When the loop is out of lock, as when the BFO receives a new command frequency, the control voltage moves to change the tank frequency thereby re-establishing lock. Correct adjustment of C42 results in the BFO control voltage being near mid-range when the VCO frequency is at mid-range, 9.5 MHz. Note that C42 can be adjusted through its range and the loop will remain locked so long as the BFO control voltage is able to maintain an opposing capacitance on the varactor.

The 8.5 to 10.5 MHz square wave output from pin 3 of U27 has ECL high and low states of about 4.1 volts and 3.3 volts, respectively. Transistor Q11 changes these to TTL levels. NAND gate U33D receives the output of Q11 and provides signal for both the loop divide-by-N stages and the loop output.

Conversion To 455 kHz. - The 8.5 to 10.5 MHz frequency from the synthesizer must be divided to provide the 445 to 465 kHz BFO frequency for the 455 kHz IF stage. To do this, 36 MHz is mixed with the 9.5 MHz to produce 45.5 MHz. Dividing the 45.5 MHz by 100 produces the required 455 kHz. These circuits are described in detail in the remaining paragraphs of the BFO circuit descriptions.

A 36 MHz signal is taken from U1B in the 2nd LO synthesizer. Line receiver U19C isolates the 2nd LO from the BFO stages. The 36 MHz differential output from the line receiver drives mixer U6D. Combining 36 MHz and 9.5 MHz in the mixer results in a sum signal of 45.5 MHz. A 4-pole LC filter at the mixer output allows only the desired 44.5 to 46.5 MHz range to be applied to line receiver U19A. Coils L13 and L14 are adjusted by monitoring pin 3 of U19A with an oscilloscope. Proper adjustment produces equal levels at the band edges, 44.5 and 46.5 MHz; and a slight peak at center frequency, 45.5 MHz.

Output from U19A gets increased to TTL levels by U19B. Transistors Q4 and Q5 form another differential amplifier to allow biasing Q6 just below turn on. This is done by setting the BFO to mid-frequency and adjusting R39 for maximum undistorted signal at the collector of Q6. When properly adjusted, R39 also provides minimum noise. Coil L8 provides for a fast pulse and diode CR8 prevents saturation of Q6.

Following Q6 are two divide-by-10 stages, U24 and U28. Their clock inputs are active on the low-going edge. Outputs are symmetrical. Both inputs and outputs are TTL compatible. A low to the reset input of U28 inhibits the data output. Their divide-by-100 action changes the 45.5 MHz to the required output of 455 kHz.

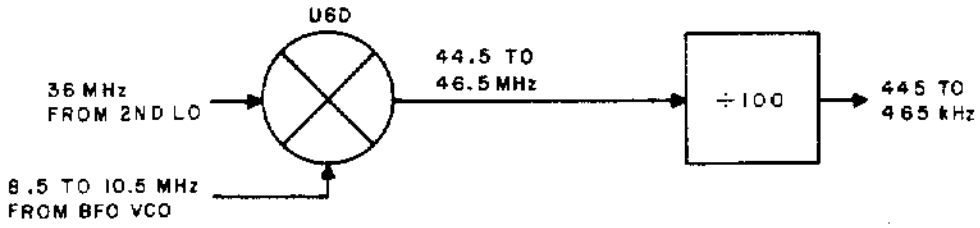


Figure 6-25. BFO VCO Conversion to 455 kHz

4.4.7 TIME BASE CIRCUITS. - Time base circuits are a part of the type 791109 board, A18. Refer to schematic diagram Figure 7-20 for the following descriptions. When the receiver operates in the internal mode all reference signals originate with the 2 MHz TCXO, U20. But an external 1 MHz source can also be supplied. When the internal reference source is used, the external reference select input, pin AU, is grounded. This pulls pin 5 of NAND U17A low and likewise, the input of inverter U16A low. The high output of the inverter, then, is applied to the active-low set-input of the type D flip-flop. A high there

establishes the condition for an output at the Q and $\overline{Q}$ terminals of the flip-flop. A 2 MHz signal from the TCXO clocks the flip-flop, and a divide-by-two action is established with the data input being coupled the $\overline{Q}$ output.

Returning to NAND U17A, the low state at pin 5 gives a low at pin 11 of U17B. Notice that the other input, pin 12, is maintained at 2.5 volts by the divider network, R27 and R28. This difference between the two inputs provides a TTL high state at the output, and NAND gate U17B then passes the 1 MHz reference signal from the flip-flop.

If an external reference is to be used with the receiver, board pin AU floats high. This gives a high state both to pin 5 of NAND gate U17A and to inverter U16A. The inverter pulls the set input of the flip-flop low, and the Q output is held high. This high state allows NAND U17B to pass the 1 MHz reference input received on the other input. It originates at the external reference input, pin AJ. From AJ the signal is applied to pin 1 of U17A, through NAND U17A, to pin 11 of U17B. NAND U17B applies the 1 MHz external reference to the dividers, beginning with U21A.

External reference input pin AJ also serves as a reference output when the time base operates in the internal mode. This signal originates with the $\overline{Q}$ output of the flip-flop and routes through a low-pass filter before connecting to pin AJ.

The basic 1 MHz reference is further processed by six other dividers and an inverter thereby providing a total of eight reference outputs. They are labelled as the time base out on the schematic. Isolation for the 250 kHz and 10 kHz second LO reference outputs is provided by U16E and U16F, respectively.

4.4.8 POWER FAIL DETECTOR. - This stage is a part of the Type 791117 circuit board. It is shown at the lower left of the schematic diagram, Figure 7-21. In essence, the detector maintains a logic high at output pin A21 unless there is a power failure. To do this, U32A acts as a comparator for voltages applied to inputs 3 and 4. Input 3 is derived from a highly regulated 5 volt source. Input 4, on the other hand, receives its voltage from the 10 volt line, which is unregulated. The 10 volts connects to the board at pin A18. Voltage regulator VR1 reduces the voltage by 6.2 volts and applies it to potentiometer R4. Voltage from the wiper of this potentiometer sets the charge voltage on capacitor C2. Under the full charge condition on C2, resistor R8 has an insignificant charge/discharge current through it, and therefore an insignificant voltage drop across it. Diode CR5 then, is not biased into conduction.

Pin 3 of U32A receives its bias voltage from a different source. Positive 15 volts connects to the board at pin AZ. Voltage regulator diode VR2 drops this incoming voltage by 3.2 volts and couples it to pin 16 of U32E. An internal regulator stage in U32E provides a 5 volt reference source at pin 9. This regulated 5 volts supplies potentiometer R6 with a stable source which is then used to set the voltage at pin 3 of U32A.

If there is either a power failure or the receiver is turned off, voltage on the 10 volt line drops faster than the voltage on the regulated 15 volt line. As the 10 volt line drops, diode CR5 becomes forward biased and rapidly discharges C2.

Lowering the voltage on pin 4 of U32A while pin 3 remains biased causes output pin 13 to go low. This low state connects to program sequencer A20 which initiates memory functions in the receiver.

4.5 DIGITAL CONTROL SECTION

All operating modes and parameters of the receiver are controlled by the digital control section. The digital control section functions by means of a circulating data stream. A sixty-four bit data word is serially transferred back and forth primarily between a shift register associated with the front panel controls and a shift register associated with the receiver section of the WJ-8888. The main memory, interrupt memory, or the remote control unit are also cycled into the data loop when it is necessary to write into or obtain information from a memory or to communicate with the remote control unit. In the local operating mode, front panel control data is loaded into the front panel shift register, then the data is shifted into the receiver register where it is loaded into storage latches for use by the receiver section. Signal strength and RF gain data is added to the data word when it is in the receiver register. The data word is then shifted back into the front panel register and also into the interrupt memory and possibly a selected main memory channel. The frequency and control data in the front panel register is read out into storage latches which illuminate the front panel controls and tuned frequency numeric display. In the memory operating mode the receiver section remains set at the most recently selected operating point, while the front panel displays the parameters clocked into the front panel register from a selected memory channel. In the remote operating mode, a data word is clocked from the remote control until to the receiver register. After the data is loaded into the receiver storage latches, the data word is transferred to the front panel register as before. The front panel controls indicate the remotely selected operating parameters and the numberic display indicates the remotely selected tuned frequency, but the controls and manual tuning dial are inoperative. The data word from the receiver shift register, which contains the signal strength and RF gain data as well as the operating parameters of the receiver, can be clocked out to the remote control unit while in any operating mode. All routing of the data word is achieved by a program sequencer circuit which controls a multiplexer and load and read functions of the memories and shift registers. The following paragraphs provide a detailed description of data-word routing in terms of timing and functional block diagrams.

4.5.1 FUNCTIONAL BLOCK DIAGRAM AND PROGRAM SEQUENCING. - Refer to the Simplified Block Diagram of the Digital Control Section, Figure 4-26. The multiplexer selects a serial data word clocked out of the front panel register, the receiver register, the main or power interrupt memory, or the remote control unit via the input/output (I/O) module, for application to the common data node. The data on the data node is simultaneouely clocked back in to one or more of these circuit sections as appropriate to recirculate the data word and load the memories as required. All timed operations, including multiplexer programming, shift register load and read functions, memory write and read functions, and I/O clocking are controlled by a program sequencer board and miscellaneous related logic circuitry distributed on the other digital control section boards.

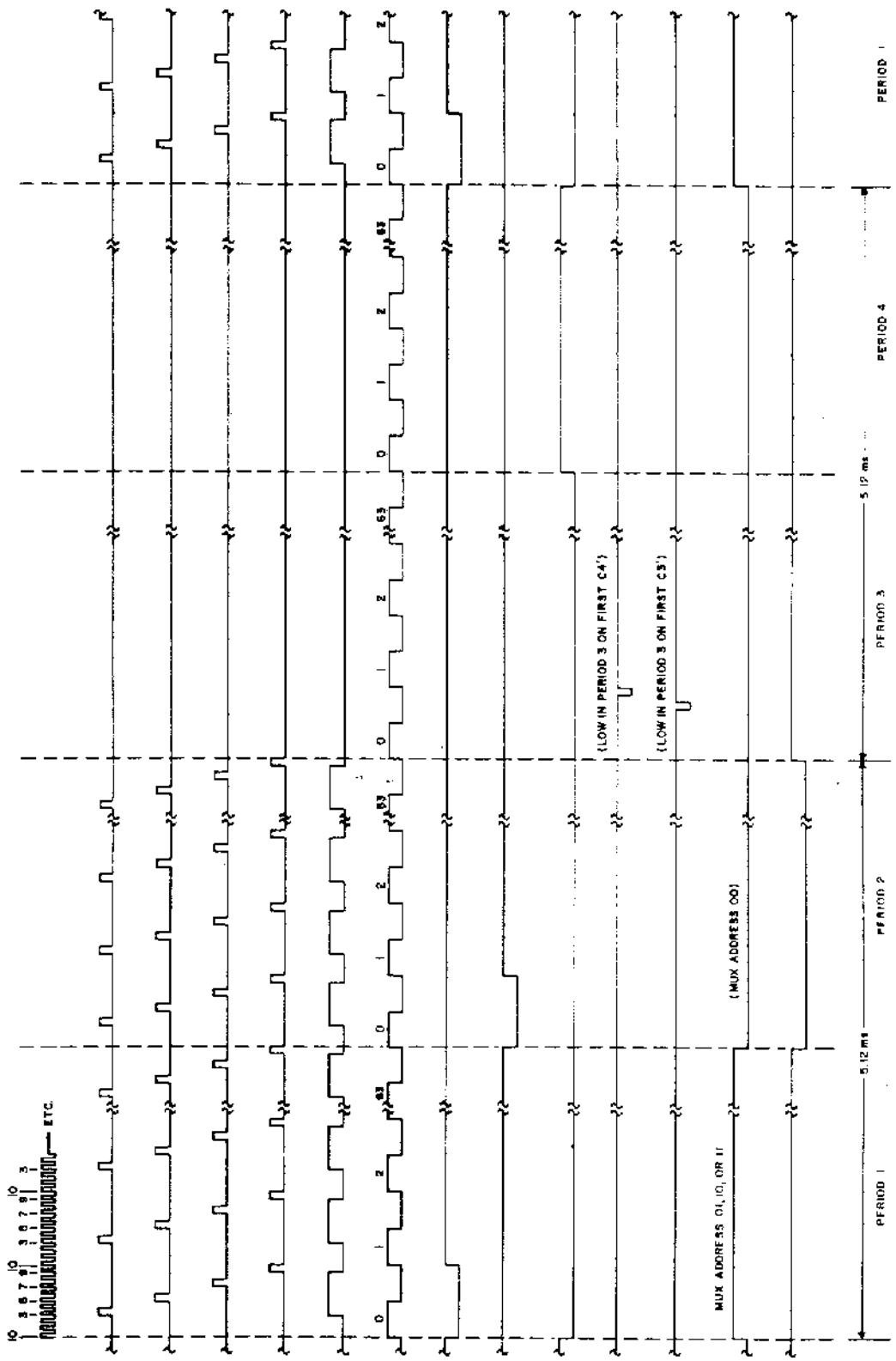


Figure 4-27. Digital Control Section, WJ-8888, Overall Timing Diagram

Program sequencing may be understood by referring both to the basic timing diagram and the table of operating modes, Figure 4-27 and Table 4-7 respectively. Note that the program cycle is divided into four equal periods, each 2.56 ms (64 25-kHz clock pulses) long. During period 1 a 64-bit data word is serially clocked into the receiver shift register from the front panel register, a memory, or the I/O module, via the multiplexer and data node. The specific period-1 data source depends on the operating mode or sub-mode in effect. During period 2 the data word in the receiver register is clocked back in to the front panel register and also possibly a memory and the I/O module, depending on the operating mode or sub-mode in effect. The receiver register is the data source for every period 2. Note that Clock 2 clocks the receiver and front panel shift registers and gates the memory Write Enable commands, and also note that the memory address changes and the memory Chip Enable command occurs before each Clock 2 pulse occurs. Clock 2, therefore, is the basic clock which transfers the data word to and from the shift registers and memories. The receiver and front panel shift registers clock on the trailing edges of Clock 2, to permit time for the memory write function to occur (leading edge of Clock 2) before data changes. In the remote active sub-mode, in period 1 while an address and remote trigger are received from the computer, Clock 3 clocks data from the remote control unit shift register to the multiplexer via the I/O module. Because bit 1 of the data word from the computer is in a ready state on interrogation, Clock 2, although it preceeds Clock 3, is able to clock the entire remote data word from the multiplexer into the receiver shift register. Similarly, during period $\overline{2}$ in any mode, Clock 1 accompanies the data to the computer, as enabled by $\overline{2}$ and if the I/O module receives an address from the computer. If Load A is determined by the operating mode to occur at the beginning of period 1, when the data word is still in the front panel register, operating parameter control information is parallel loaded into the shift register to update the data word. Similarly, if Load B is programmed to occur at the beginning of period 2 when the data word is still in the receiver register, signal strength and RF gain data is parallel loaded into the shift register (or in remote active mode RF gain data is read from shift register) and also tuned frequency and operating mode data is read from the shift register to update the receiver storage registers. Following period 2, when the data word is in the front panel register, two periods occur in which the clocks are inactive. The End-Of-Cycle (EOC) pulse which occurs in period 3 commands the pushbutton lights and tuned frequency numeric display to update with the latest operating status and frequency of the receiver. Load C occurs only on the first cycle following return to local operation from memory or remote modes, or on return to remote operation from power failure. Load C commands switch encoder latches and the tuning dial up/down counter to preset with information from a data word obtained from the interrupt memory, so that the unit resumes operation on the next period 1 from a predetermined starting point. Mode change occurs in period 4, and is prevented from changing during periods 1, 2, and 3 to avoid scrambling of information on the data word.

Referring to Table 4-7, note that there are three main operating modes, three corresponding sub-modes, and a local/remote return sub-mode. Specific mode and multiplexer address codes occur for each of these modes, whether

Table 4-7. Operating Modes

MODE	MODE CODE ⊙ 2^2 A	2^1 B	2^0 C*	PERIOD 1 △ MUX 2^1	ADDRESS 2^0	MUX DATA SOURCE	LOAD A	B	C	MAIN MEMORY □ CHIP ENABLE 1	2 ✿	WRITE ENABLE 1	2 ✿	INTERRUPT MEMORY □ CHIP ENABLE 1	2 ✿	WRITE ENABLE 1	2 ✿
Local	1	1	1	0	1	F.P. Register	1	1	0 +	0	0 +	0	0 +	0	1 +	0	1 +
Memory Write (Enter)*	1	1	0	0	1	F.P. Register	1	1	0	1	0	1	0	0	1	0	1
Remote (Passive)	0	1	1	0	1	F.P. Register	0	1	0	0	0	0	0	0	0	0	0
Remote (Active)*	0	1	0	1	1	I/O Module	0	1	0	0	0	0	0	0	1	0	1
Memory Scan	1	0	1	1	0	Memory	0	0	0	1	0	0	0	0	0	0	0
Memory Execute*	1	0	0	1	0	Memory	0	1	0	1	0	0	0	0	1	0	1
Local/Remote Return★	Return			1	0	Memory	0	1	1	0	0	0	0	1	1	0	1

* C high indicates major mode;
C low indicates sub-mode of corresponding major mode.

* Mode automatically returns to local after memory write sub-mode cycle, automatically goes through L/R return sub-mode cycle and then returns to local mode after memory execute sub-mode cycle, or automatically returns to remote passive mode after remote active sub-mode cycle when remote trigger is removed.

★ One L/R return sub-mode cycle occurs before unit goes to major mode when LOCAL button is pressed while in memory or remote mode, on return to local after memory execute sub-mode cycle, or when returning to remote mode from power failure.

\+ 1 = occurs, 0 = does not occur

✿ 1 indicates 1st period, 2 indicates 2nd period, of 4-period program cycle.

□ Chip-enable with no write-enable indicates read function. Write enable occurs on clock 2.

△ Period 1 only. Multiplexer address is 00 on every period 2. (Receiver register is data source when multiplexer address 00)

⊙ Mode can change only during period 4.

manually or automatically selected. These codes determine multiplexer data source, and whether or not Load A, B, C, and Memory Chip and Write Enable commands occur during periods 1, 2, or 3 of the program cycle. This table and the basic timing diagram may be used as aids in determining specific program cycling for the operating modes and sub-modes as follows:

(A) LOCAL Mode. -

(1) Period 1, Data Source Front Panel Register. -

(a) A Load A command at the beginning of period 1 parallel teansfers front panel data into the F. P. shift register. Synchronous loading on the first Clock 2 pulse moves data ahead 1 position as it is loaded. Locked Load A permits the BFO A/D converter output to be loaded only when not in the BFO VAR mode or following the first press of the CW VAR button if in the BFO VAR mode. The CW VAR button flashes the first time it is pressed and released, indicating that the variable control may be used to set the BFO frequency. The light becomes steady the second time the button is pressed and released, indicating that the control is no longer effective and that the BFO code in the shift register does not change and is that most recently set by the control (see also memory execute sub-mode description). In detection modes other than BFO VAR, the A/D converter output data word is fixed at 0. See the operating instructions in Section 2 or the appropriate schematic description for other internal restrictions on the front panel controls. Logic 0 is loaded into the AGC dump position. (AGC dump operated by remote control only.)

(b) 64 Clock 2 pulses transfer the data word, via the multiplexer and data node, to the receiver register (and also back to the F. P. register). The data word already in the receiver register is clocked out and not used. The interrupt memory and the I/O module remain disabled. The main memory remains disabled unless the ENTER button was pressed during the most recent period 4.

(c) (MEMORY WRITE Local Sub-Mode only.) - ENTER button illuminates first time pressed. The second time ENTER button is pressed, the button light goes out and the main memory channel selected with the thumbwheel switch becomes enabled by Chip Enable Main during period 1. Write Enable Main also occurs to clock the front panel register data word into the selected memory channel during period 1, replacing existing information in that channel. The Memory Write sub-mode occurs only once, and in period 4 the unit automatically returns to the normal local mode.

(2) Period 2, Data Source Receiver Register. -

(a) The leading edge of the Load B command loads the receiver storage registers and updates the signal strength and RF gain A/D converters. BFO select data is loaded if the detection mode word most significant bit (MSB) is logic low.

If the MSB is high, a fixed word (10000000000) is loaded (see data word diagram in section III).

(b) The first Clock 2 pulse of period 2 occurs, moving data ahead one bit to properly position the 2 spare bits following the RF gain and signal level words (see data word diagram).

(c) The trailing edge of Load B parallel loads signal strength and RF gain data into the receiver shift register.

(d) Each trailing edge of Clock 4 clocks the preselector decoding circuit. (As many as 16 Clock 4 pulses may be required to update this circuit - refer to the schematic description for details.)

(e) 64 clock pulses of period 2 transfer the receiver register data word, via the multiplexer and data node, to the F.P. register, I/O module, and interrupt memory (and also back to the receiver register). Old data is clocked out of the F.P. register and not used. The Chip Enable signal permits the interrupt memory to update with the latest receiver signal strength, gain, and operating parameter codes during this period. The main memory is disabled in this period, however.

(f) $\overline{2}$ permits the data word applied to the I/O module to be passed on to the remote control unit if an address is received (see Serial Synchronous Timing Diagram, Figure 4-28). Clock 1 accompanies the output data word from the I/O module for use by the remote control unit in clocking the word into the remote control unit shift register. (Note that the first data bit is active at the beginning of period 1, so that is is necessary for the first clock pulse sent to the remote control unit (Clock 1) to preceed the first Clock 2 pulse.)

(3) Periods 3 and 4. -

(a) The clocks are stopped, so that the data word remains in the front panel register. The memories and I/O module are disabled.

(b) The End-Of-Cycle (EOC) pulse loads detection mode, IF bandwidth, and gain mode data from the front panel shift register into storage latches. The storage latches in turn operate a pushbutton lighting circuit and also provide detection mode data to the BFO A/D converter circuit. The EOC pulse also updates the front panel numeric display with the most recent tuned frequency data.

(c) Receiver operating mode may change during the fourth period. The desired mode button may have to be held down for a maximum of three time periods (7.68 ms), which is faster than operator reaction time. (See LOCAL/REMOTE RETURN sub-mode discussion below for description of Load C.) In all cases change from a sub-mode to a major mode occurs automatically at the beginning of period 4.

(B) REMOTE PASSIVE Mode. -

(1) Period 1, Data Source Front Panel Register. - 64 Clock 2 pulses transfer the data word in the F. P. register, via the multiplexer and data node, to the receiver register (and also back to the F. P. register). Interrupt and main memories are disabled. Load A does not load front panel data into the F. P. register during this period.

(2) Period 2, Data Source Receiver Register. - Essentially the same as for the local mode, the differences being as follows:

(a) The local/remote status line causes the RF gain converter to function in the D/A mode. The leading edge of Load B, therefore, instead of updating the A/D converter with RF gain data based on the setting of the RF GAIN potentiometer, updates the D/A converter with gain control data obtained from the data word. (The D/A converter RF gain data is clocked back into the receiver register on the trailing edge of Load B as for the local mode; however, this operation, which results in no net change, will have meaning in this case only if reference is made to the specific operating principle of the A/D-D/A converter, covered in the appropriate schematic description below.)

(b) The interrupt memory is disabled.

(3) Periods 3 and 4. - Same as for local mode.

(C) REMOTE ACTIVE Sub-Mode. -

(1) Period 1, Data Source I/O Module. - The remote trigger (see Figure 4-28) and L/R status signals permit 64 Clock 3 pulses to clock a data word from the remote control unit (or from I/O shift register if asynchronous I/O option is installed). The data word received on the data node via the I/O module and multiplexer is entered into the receiver shift register (and also F. P. register) by Clock 2. Bit 1 from the remote control unit (always 0 because not used) is available on address, which therefore requires that the DATA IN clock (Clock 3) follows Clock 2. Both memories are disabled during period 1 in this mode.

(2) Period 2. - Same as for local mode except modification described in step (2a) for remote passive mode applies, and if an AGC dump command was clocked in during period 1 the AGC circuit in the receiver section will be reset.* Note that the interrupt memory is updated and receiver register data is returned to the remote control unit in this period.

(3) Periods 3 and 4. - Same as for local mode. The unit automatically reverts to the remote passive mode (at the beginning of period 4) for the next program cycle.

* AGC Dump may not be functional in earlier models.

(D) MEMORY SCAN Mode. -

(1) Period 1, Data Source Main Memory. - Main memory chip enable signal and bit address code permit 64 Clock 2 pulses to shift the data word stored in the main memory channel selected by the front panel thumbwheel switch, into the receiver register (and also into the front panel register). Memory readout is non-destructive. The data word already in either register is clocked out and not used. The I/O module and interrupt memory remain disabled.

(2) Period 2, Data Source Receiver Register. - 64 Clock 2 pulses transfer the data word from the receiver register, via the multiplexer and data node, to the F.P. register (and also back to the receiver register) (The same data word already in the F.P. register is clocked out and not used.) Load B does not occur, so the data word is not updated with signal strength or RF gain data, and the receiver operating mode does not change. While in the memory scan mode, the MEMORY button flashes as a reminder that the front panel data may not represent the actual operating status of the receiver.

(3) Periods 3 and 4. - Same as for the local mode.

(E) MEMORY EXECUTE Sub-Mode (Executed while in Memory Scan Mode Only). -

(1) Period 1, Data Source Main Memory. - EXECUTE button lights while held down. In period 1 the main memory chip enable signal and bit address code permit 64 Clock 2 pulses to shift a data word from the selected main memory into the receiver register (and also into the front panel register). Memory readout is nondestructive. The I/O module and the interrupt memory remain disabled.

(2) Periods 2, 3, and 4. - Same as for the local mode. Unit reverts to local mode (after return sub-cycle) when execute submode is completed. BFO Load A is locked on return to local to disable the VAR BFO control so that, if the detection mode data stored on the data word is BFO VAR, in the next period 1 the receiver remains programmed with the variable BFO frequency stored in the selected memory.

(F) LOCAL/REMOTE RETURN Sub-Mode. - The unit first goes through a local/remote return sub-mode cycle when the LOCAL button is pressed while in the memory or remote mode, when returning to local after a memory execute sub-cycle, or when returning to the remote mode from power failure. It does not go through a return sub-cycle after a memory enter sub-cycle.

(1) Period 1, Data Source Interrupt Memory. Interrupt memory chip enable signal and bit address code permit 64 Clock 2 pulses to shift the data word stored in the interrupt memory into the receiver register (and also the front panel register). Memory readout is non-destructive. The I/O module and main memory remain disabled.

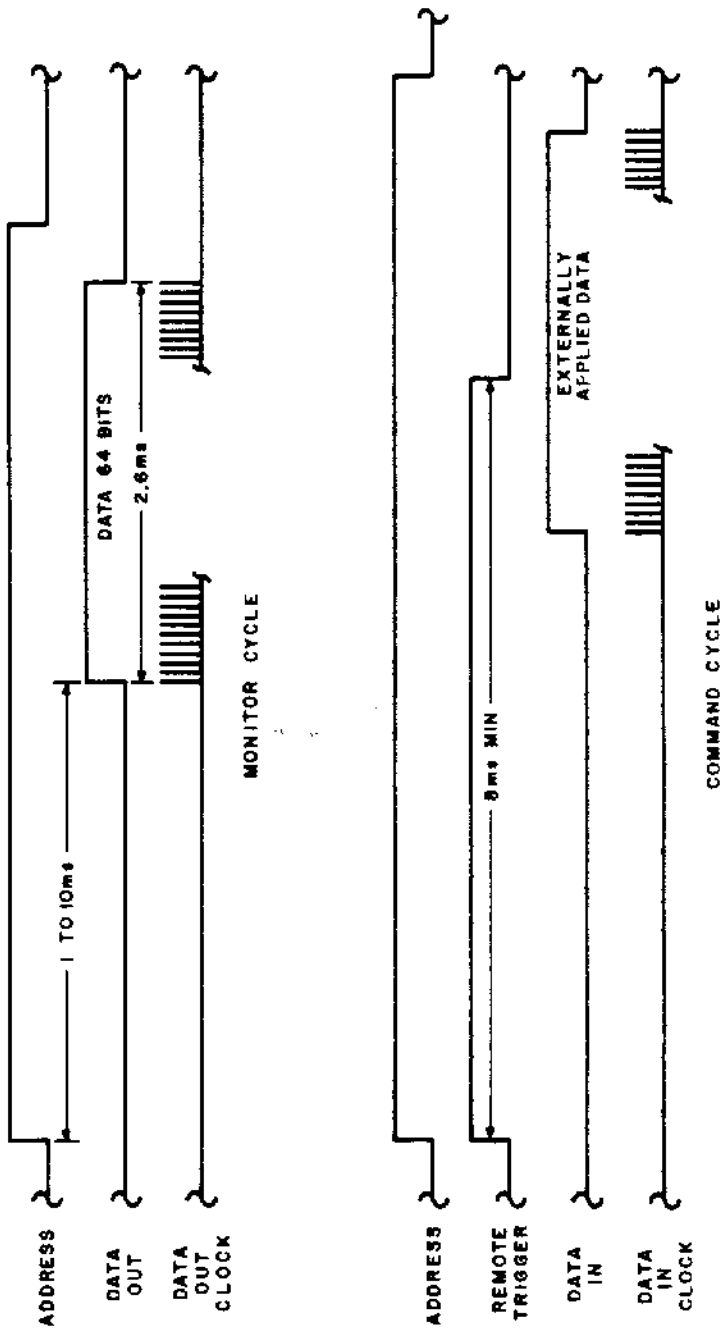


Figure 4-28. Serial Synchronous I/O Timing Diagram

(2) Period 2, Data Source Receiver Register. - Same as for local mode.

(3) Periods 3 and 4. - Steps (a), (b), and (c) same as for local mode. Continue with step (d) as follows:

(d) Load C presets the switch encoder latches and the tuning dial up/down counter with the data word obtained from the interrupt memory, so that the unit resumes local or remote operation on the next period 1 from a starting point determined by the contents of the interrupt memory, which is in turn determined by the most recent receiver operation programmed by the remote control unit, by the selected main memory, or most recent local selections. Note: The unit always returns to the remote mode from power failure. If another operating mode was in effect before power failure, the unit can be restored to that mode by pressing the appropriate front panel button. The unit will then resume operation at a point identical with that preceeding power failure.

4.5.2 SCHEMATIC DESCRIPTIONS. - The digital control section circuitry is distributed on six boards, these being called the Program Sequencer Board (A20), the Front Panel Register Board (A22), the Switch Encoder Board (A21), the Receiver Register Board (A17), the Display/Buffer Board (A23), and the I/O Module (A16). In addition, a Tuning Dial Encoder Assembly (A25), a memory-select thumb-wheel switch (S5), and an Optional Tuning Connector Filter (A24) are also considered part of the digital control section. The introductory paragraph of each of the following board description summarizes the circuits situtated on the board, permitting the functional block diagram description to be keyed to the circuit descriptions. In addition, the overall main chassis diagram, Figure 7-33, may provide useful references.

4.5.2.1 Type 791124 Program Sequencer Board (A20). - Refer to the schematic, Figure 7-22. The program sequencer board contains most of the programming circuitry for the digital control section. Some of the logic operations are completed by front panel switches and logic circuitry located on other boards. The program sequencer generates the four clocks (C1, C2, C3, and C4), the memory address code, End-Of-Cycle (EOC), Load A, Load B, and Load C commands, multiplexer address and local/remote (L/R) status signals, $\overline{2}$ for the I/O module, and develops the majority of the write enable and chip enable signals for the memories. These logic functions are controlled by a mode code (see Table 4-7) developed on this board in conjunction with the front panel switches, located on the switch encoder board (A21), and the remote trigger input from the I/O board (A16). A major part of the power-down circuit is also located on this board.

Gated Clock and Memory Address Circuits. - Decade counter/divider U1 divides the 250 kHz time base clock, received on board pin B19 from the synthesizer section of the receiver, by 10 to provide a 25 kHz memory address increment output to binary counter U9. U1 also produces four un-gated 25 kHz clock outputs (designated by prime " ' " superscripts), C1' through C4', having a phase relationship identical to the four gated clocks shown on the basic timing diagram,

Figure 4-27. The inverted 2^7 gating pulses received on one input each of NAND gates U8 A through D, from memory address counter U10A via inverter U11C, permits clock pulses to pass through NAND gates U8 A through D in program cycle periods 1 and 2, but inhibits these clocks in periods 3 and 4. U29A through D invert the U8 outputs to cancel the inversions caused by U8. The gated outputs are distributed as follows: $\overline{C2}$ on board pin B17 is applied to the receiver register board, C1 on pin B13 is applied to the I/O board, C2 on pin B18 is applied to the front panel register board, C3 on pin B14 is applied to the front panel register and I/O boards, and C4 on board pin B12 is applied to the receiver register board. C3', C4', C2, C1, and C4 are also used for various logic functions on this board.

U11E inverts the carry out pulses of the clock counter, so that negative-edge-triggered binary counter U9 increments simultaneously with the trailing-edge transition of each Clock 4 pulse (see timing diagram). Binary counters U9 and U10 are cascaded to provide a binary sequence from 2^0 to 2^7. The 2^0 through 2 outputs are applied to various logic gates on this board to help generate the program sequence. The 2^0 through 2^5 counter outputs are also applied directly to the front panel register board for use as the Memory Address code. The chip enable (CE) input of U1 and the data strobe (DS) inputs of U9 and U10 are covered below in the power fail circuit description. For this description, however, assume that the receiver is operating normally, in which case pin 5 of U11B is low and pin 4 is high, permitting U1, U9, and U10 to function normally as counters.

Program Logic Circuit. - The array of logic gates and inverters to the right of U10 and U16 A, B, & C combine the U9-U10 counter output and some of the clock outputs with mode logic functions generated by the remaining logic circuitry on this board, to produce program sequence logic outputs. The 2^2, 2^1, and 2^0(A, B, and C) mode code inputs to this array are obtained from U12A, U13A, and U16A, respectively. This circuit need not be analyzed in detail, since it produces its results by straightforward gating and inverting operations which are easily traceable by a two- or four-trace oscilloscope if a malfunction occurs. The outputs from this board are distributed as follows: The $\overline{EOC}$ output (pin C4) is applied to the switch encoder board and I/O module. $\overline{Load\ A}$ (pin A9) is applied to the front panel register, $\overline{Load\ C}$, (pin AD) is applied to the switch encoder, $\overline{Load\ B}$ (pin AE) is applied to the receiver register, Load D (pin AT) is not used, the L/R Status output (pin A20) is applied to the receiver register and I/O module, the Multiplexer Address (pins A19 and A22) is applied to the receiver register board and I/O module, $\overline{2}$ (pin B4) is applied to the I/O module, and outputs designated $\overline{CSS}$, X1, X2, $\overline{CSI}$, and $\overline{CSE}$ (pins A8, A18, A21, AM, and A7, respectively) are applied to the front panel register. The latter five outputs are combined on the front panel register board to form Chip and Write Enable signals for the main and interrupt memories. The functions of the former outputs, as well as chip and Write Enable signals are covered in the simplified functional block diagram and timing diagram descriptions above (paragraph 4.5.1).

Mode Code Circuit. - The program logic circuit is controlled by the mode code circuit. The two most significant mode code bits (board pins A3 and A7) also help operate the pushbutton lighting circuit on the switch encoder board.

The mode code is initiated by the front panel pushbuttons or the remote trigger input from the I/O module. With appropriate inputs from the pushbutton switch, program logic, and power return circuitry, NAND latches U12 A-B and U13A-U7C produce the major mode code bits (2^2 or A and 2^1 or B, respectively), NAND latches U12C-U13B and U31A-B, together with gates U32A, U32B, U3C, and inverter U16A, produce the sub-mode bit (2^0 or C), and NAND latch U31C-U7D produces an output which causes the program to go through a local/remote return sub-mode cycle. NAND gates U4B, C, and D, U6 C and D, and U7A are controlled by a mode change pulse (see timing diagram), such that inputs to the latches originating from the front panel switch and remote trigger circuitry are able to change the operating mode only during program cycle period 4. The mode Change pulse is generated by the NOR combination of inverted 2^6 and 2^7 outputs from counter U10. Note, however, that EOC sub-mode reset pulses and power fail preset levels applied to the latches from U17D and U2A, respectively, are not gated by the Mode Change pulse. For the following description of the dynamics of the mode code latches, assume that the receiver is operating normally, such that the $\overline{Q}$ output of power fail latch U2A is high, enabling NAND gate U7B and permitting the various NAND latches to which the output is connected to be operated by their other inputs. Also, therefore, during normal operation the Q output of U2A will be low, permitting NOR latch U30C-U20C and flip-flop U2B to operate normally as part of the execute sub-mode circuit.

The following considerations establish an initial starting point for the description which follows: With no front panel pushbuttons pressed and with no remote trigger input, the outputs of U4 B, C, and D, U6C, and U7A are all at logic high. If during a program cycle the Enter sub-mode is active (to be described below), during period 4 of the cycle preceeding the sub-mode cycle, NAND latch U12C-U13B changes state. This causes one-shot MV composed of U14C, U16 B & C, C13, CR2, and R1 to generate a pulse which immediately resets flip-flop U5 of the memory write sub-mode circuit. The resultant logic low output from pin 13 of U5B disables U6D so that the output of U6D is at logic high. The logic high permits the $\overline{EOC}$ pulse to return the unit to a major mode during period 3 of this or any subsequently initiated sub-mode cycle by setting up NAND latches U12C-U13B and U31 A-B, as well as NAND latch U31C-U7D, such that U12C pin 10, U31A pin 9, and U31C pin 10 are all at logic low. Also, in any mode or sub-mode except the Execute sub-mode cycle (which will be described below), the middle and least significant mode code bits (see Table 4-7) applied to U30B are such that pin 9 of U30C is held low. This permits the EOC pulse, inverted by U11F, to reset the Execute-local return circuit (U20C, U30C, U2B), such that the output of U2B (pin 13) is high, enabling NAND gate U4A. (See power-fail latch description below for discussion of function of CR3.) A starting point is now established which will support the following description of the dynamics of the mode code circuit; the memory write and execute-local return circuits which were briefly mentioned here are described in detail below.

Assume that the LOCAL button is pressed, causing a logic low (ground) on board pin C13 while the button is held down. U4A inverts the low, enabling NAND gate U4B. The resultant logic low output from U4B in period 4 sets up NAND latches U12 A-B and U13A-U7C such that U12A pin 9 (mode code 2^2 output)

is high, and U13A pin 1 (mode code 2^1 output) is high. Since the combination of logic levels applied to exclusive OR gates U32A and U32B is now that necessary to result in a logic high at pin 2 of U16 (mode code 2^0 output), the overall mode code is that indicated for the Local mode in Table 4-7. However, the program logic circuit is not yet able to operate the unit in the Local mode because the logic low output in period 4 from U4B also sets up NAND latch U31C-U7D such that pin 10 of U31C is high. The high output from pin 10 of U31C, applied to U21A, U16D, U22A, etc. of the program logic circuit causes the program logic circuit to produce a Local return command during periods 1 and 2 of the next cycle (see Table 4-7). NAND latch U31C-U7D is reset by the $\overline{EOC}$ pulse in period 3 of the local-return sub-cycle, so that the program logic circuit is permitted to produce major local mode control codes for succeeding cycles. (The logic high transition from U31C pin 10 at the beginning of the return sub-cycle also causes the one-shot MV circuit to produce a negative pulse output, which is inverted by U7B and applied to the reset inputs of U5 A & B. In this case the reset pulse is not necessary, since U5 was reset prior to an enter sub-cycle, as described above. But on return to the Remote mode from power failure it is necessary to preset U5 during the return sub-cycle. This will be discussed below in the power-fail circuit description.)

The ENTER button is disabled when not in the Local mode, as will be discussed in the switch encoder schematic description. When the ENTER button is disabled, pins 1 and 6 of U6 are at logic high. When in the Local mode, however, if the button is not depressed pin 1 of U6 is high and pin 6 is low. Pin 3 of U6A is therefore low and U5A is not clocked. Initially assuming that U5A and U5B are reset as described above. In the reset condition the Q1 (pin 1) output of U5A is low, so that the ENTER pushbutton does not illuminate, the $\overline{Q1}$ (pin 2) output of U5A is high, and the Q2 (pin 13) output of U5B is at logic low and disables U6D as described above. If the ENTER button is pressed and then released, pin 1 of U6 momentarily goes low and pin 6 momentarily goes high. Pin 3 of U6A follows the pushbutton action by momentarily going high, although without the bounce characteristic of pushbuttons. U5A is clocked by the high transition of de-bounce NAND latch U6A. The Q1 (pin 1) output of U5A goes high and illuminates the ENTER pushbutton lamp. The low transition of the $\overline{Q1}$ output (U5A pin 2) does not change the state of U5B because U5B requires a positive clock transition. The second time the ENTER button is pressed, however, U5A again changes state, extinguishing the ENTER button lamp and producing a positive Q1 transition which clocks U5B. The Q2 (pin 13) output from U5B therefore goes high and enables NAND gate U6D, permitting the Mode Change pulse to be gated through U6D on the occurence of the next period 4. At the beginning of period 4, the logic low output from U6D changes the states of sub-mode NAND latches U12C-U13B and U31 A-B, such that pin 10 of U12C and pin 9 of U31A go high. The high transition of U12C causes the one-shot MV circuit to produce a pulse output which immediately resets U5 A & B. The four high inputs to NOR gates U32 A & B, from the major and sub-mode latches, result in a logic low output from U16A. Therefore, the overall mode code is that indicated in Table 4-7 for the Memory Write sub-mode. Note that the inputs to the sub-mode logic gates are set up so that an enter command will not produce a sub-mode

bit unless the unit is in the major Local mode. This safety feature is redundant, however, with the disabling of the ENTER button when not in the Local mode. After one Memory Write sub-cycle, the EOC pulse resets sub-mode latches U12C-U13B and U31 A-B so that the unit returns to the major Local mode.

When the MEMORY button is pressed, board pin C12 goes high, enabling NAND gate U4C so that it passes the Mode Change pulse in the next period 4 while the button is held down. The logic low output from U4C sets up the two major mode NAND latches (U12A-B, U13A-U7C) so that U12A pin 9 is high and U13A pin 1 is low. Also, in period 3 the three minor mode latches, U12C-U13B, U31 A-B, and U31C-U7D, were reset so that the unit is not in the L/R return mode and U12C pin 10 and U31A pin 9 are low. The inputs to exclusive OR gates U32A and U32B are therefore such that the output of U16A is logic high. The overall mode code is thus that indicated in Table 4-7 for the Memory Scan mode. (The Memory Scan mode code returned to the switch encoder board causes the MEMORY button light to flash.)

If the memory EXECUTE button is pressed, board pin C16 goes high (and the EXECUTE button illuminates) while the button is held down. U7A is therefore enabled, and on the next period 4 the Mode Change pulse is gated through U7A to set up the sub-mode latches such that pin 10 of U12C is high and pin 9 of U31A is low. If and only if the unit was in the Memory Scan major mode when the EXECUTE button was pressed, the combination of logic levels applied to exclusive OR gates U32A & B is now such that the output of U16A is low. The overall mode code is thus that indicated in Table 4-7 for a Memory Execute sub-mode cycle. The middle and least significant bits of the mode code, applied to U30B of the execute-local return circuit, causes the output of U30B to go high during the Memory Execute sub-mode cycle. This high resets a circuit on the switch encoder board (necessary if detection mode in selected memory channel is BFO VAR) to prevent Load A from initially loading VAR BFO control data when the unit returns to local on the next cycle, and also changes the state of NAND latch U30C-U20C such that pin 10 of U30C is low. This low is clocked through U2B by the next EOC pulse, and causes the output of U4A to go high. U4B is thus enabled so that in period 4 the Mode Change pulse initiates a Local Return sub-cycle, after which the unit goes to the major Local mode in the same manner as when the LOCAL button is pressed. NAND latch U30C-U20C and flip-flop U2B are reset by the EOC pulse in period 3 of the local-return submode cycle.

If the REMOTE button is pressed, board pin C11 goes high and enables NAND gate U4D. The period 4 Mode Change pulse is therefore able to set up major mode latches U12 A-B and U13A-U7C such that U12A pin 9 is low and U13A pin 1 is high. Since the sub-mode latches were reset by the $\overline{\text{EOC}}$ pulse in period 3, the combination of logic levels applied to exclusive OR gates U32A and U32B is such that the output of U16A is high. Therefote, the overall mode code is that indicated in Table 4-7 for the Remote Passive mode. If the receiver receives a remote trigger from the remote control unit, board pin C17 goes high, enabling NAND gate U6C. The next period 4 Mode Change pulse is therefore able to set up minor-mode latches U12C-U13B and U31 A-B such that pin 10 of U12C is high and pin 9 of U31A is low. If and only if the unit was already in the Remote Passive mode, the combination of logic levels applied to exclusive

OR gates U32A and U32B is such that the output of U16A is high. Now the overall mode code is that indicated for the Remote Active sub-mode. When the remote trigger is removed, the next period 3 EOC pulse resets the sub-mode latches, and the unit reverts to the Remote Passive major mode.

Power Down Latch Circuit. - While the receiver is operating normally, the power down input level from the power down detector in the synthesizer section, received on pin 5 of data-type flip-flop U2A via board pin C3, is at logic low. The (inverted) Mode Change pulse received every period 4 on pin 2 of U3A permits the 250 kHz system clock, received on pin 1 of U3A from the synthesizer section via board pin B19, to clock data-type flip-flop U2A for the duration of each period 4. Therefore, as long as the power fail input remains low the U2A Q1 output remains low and the $\overline{Q}1$ output remains high. The Q1 logic low output, applied to board pin C1, permits the I/O module and the memory chip enable circuits to function normally as described in the appropriate circuit and block diagram descriptions. This logic low is also applied, via forward-biased diode CR1, to U1, U2B, U20C, and U9 and U10 via inverter U11B, permitting these circuit components to function normally as described above. The logic high $\overline{Q}1$ output from U2A permits mode NAND latches U12 A-B, U13A-U7C, and U31C-U7D to be operated by their other inputs as described above, enables NAND gate U7B so that U7B functions as a simple inverter for enter sub-mode circuitry reset pulses, and permits NAND latch U25B-U26C of the chip enable logic circuit to be operated by clock pulses C1 and C4.

If the power-down detector senses a power failure, board pin C3 goes high. This high is independent of primary power since it is supplied by the battery (V_{DO2}) via R2. The detection of power failure is based on a drop in the +10 V unregulated power supply output. When power fails, the +10 V supply voltage drops off gradually at a rate determined by the size of filter capacitors and the drain on the supply. This permits the 5 V regulator output, which supplies the majority of the receiver circuitry including the digital control section, to continue providing regulated +5 V until some time after the unregulated supply voltage begins to drop. The point at which the power-down detector output goes high allows at least one program cycle to occur before the voltage of the regulated supply begins to drop, thus allowing time for the completion of the existing program cycle so that the interrupt memory is properly loaded. The power-down logic high is clocked through data flip-flop U2A on the occurence of the first period-4 mode-change pulse after the power-down detector changes state (or immediately by a system clock pulse if the power down circuit changes state during period 4). The logic high output from U2AQ1 immediately interrupts I/O board monitor clock and output data, and disables the interrupt and main memories on the front panel register board (see appropriate schematic descriptions). Diode CR1 becomes reverse biased when the regulated supply voltage drops, permitting the disable and preset inputs in common with the junction of CR1 and R11 to go to logic low when the regulated supply voltage drops sufficiently. The $\overline{Q}1$ output of U2A goes low when the power fail latch changes state. This low and the voltage at the junction of CR1 and R11 will be used for preset purposes when the power comes back up.

When power fails the output of U2B goes high, while a diode in U4A provides a low-impedance path to ground to protect the CMOS input. Diode CR3, situated between U2B and U4A, becomes reverse biased on power failure, thereby preventing drain on the battery by U4A (U2B is powered by the battery, which is not necessary for this part of the circuit. However, U2B is the twin of U2A, which must remain active on power failure.) Similarly, diode CR1 becomes reverse-biased on power failure to prevent drain on the battery through low-imedance paths provided by internal protective diodes at the inputs of the circuit elements connect to the junction of CR1 and R11. In normal operation resistors R11 and R12 provide forward-bias current paths for CR1 and CR3 on logic low. R12 performs a hold-up function on logic high, such that CR3 becomes reverse biased and +5 V is applied to U4A via R12.

When the receiver is de-energized, either by the operator or by power failure, the battery continues to supply the power fail latch on this board and the memories and chip enable gates on the front panel register board. Since the power fail latch only reverse biases a diode in the I/O module, since the power fail latch output applied to the chip enable gates holds them in the disable state, since CR1 and CR3 are reverse biased, and since U2, the chip enable gates, and the memories are low-drain CMOS types, the power drain is very small.

When primary power returns, the regulated supply voltage comes back up to +5 V before the unregulated supply reaches the level required to return the power fail detector output to logic low. Therefore, the junction of CR1 and R11 follows the regulated supply voltage via R11, and goes high. This high presets clock counter U1 to zero, presets memory address counters U9 and U10 such that the 2^6 and 2^7 outputs are high, and resets the execute-local return circuit such that U30C pin 10 and U2B pin 13 (Q2 output) are high. The logic low $\overline{Q}1$ output from U2A presets NAND latches U12 A-B, U13A-U7C, and U31C-U7D to ensure that the unit goes through a return sub-mode cycle and then reverts to the remote mode when the counters are enabled. The U2A $\overline{Q}1$ logic low is also inverted by NAND gate U7B to reset enter sub-mode circuit flip-flop MV's U5A and U5B, and inhibits the chip select signals by presetting NAND latch U25B-U26C.

The memory address counter preset 2^6 and 2^7 logic high outputs are combined by NOR gate U3B, and the resulting mode change high is inverted by U11A to enable NOR gate U3A. Therefore, on the first system clock pulse after the power-down detector output goes low, the Q1 output of U2A goes low and the $\overline{Q}1$ output goes high. The logic high $\overline{Q}1$ output now permits the NAND latches and gates to which it is connected to operate normally as described above. The logic low Q1 output permits the I/O module and memories to operate normally, permits the clock counter to start counting from zero, and enables the memory address counters such that the program cycle starts at the preset period 4. As determined by the mode latch preset described in the preceeding paragraph, in the first period 1 the unit goes through a return sub-mode cycle and then reverts to the major remote mode in the next period. The operator can then select a local operating mode if he so desires.

4.5.2.2 Type 791134 Front Panel Register Board (A22). - The front panel register board contains the front panel shift register, a BFO A/D converter circuit, a tuning dial sense circuit, a tuning dial up/down counter with end-point recognition circuit, and the main and interrupt memories. The power-down battery is also located on this board. Figures 7-24 and 7-25 are the schematic diagrams for A22.

Main and Interrupt Memories. - Integrated-circuit U2 is a 64-bit random-access CMOS memory, and U3 through U6 are 256-bit random-access CMOS memories. U2 is employed as the interrupt memory, while U3 through U6 are each programmed to serve as four 64-bit channels of the main memory, for a total of 16 main memory channels. The 64-bit data word from the data node (board pin B15) is applied in common to all five memory chips via NAND gate U9A and inverter U16C. U9A receives a gating input which permits application of input data to the memories only during program cycle periods in which Write Enable occurs (to be discussed further below). The data outputs (Do) from the memory chips are wire-OR'ed together for application via board pin CH to the multiplexer on the receiver register board. Resistor R30 is a pull-up resistor for the data outputs.

The incrementing binary-code memory address outputs of the program sequencer board, received on pins BS, CA, CB, CC, and CD of this board, are applied in parallel to the A0 through A5 address inputs of all five memory chips. The address code increments at a 25 kHz rate cyclically from binary 0 through 63, for a total of 64 memory bits addressed every period. Address inputs A6 and A7 of the main memory chips are obtained via U43 from the two least significant bit outputs (2^0 and 2^1) of the front-panel channel-select thumbwheel switch, and are coordinated with the chip-enable inputs to generate a total of 16 memory locations. This coordination is achieved by use of binary decoder U1, which decodes the two most significant bit outputs of the channel-select thumbwheel switch (board pins C9 and C12) into four chip-enable outputs. The chip-enable outputs are inverted by U8 A, B, E, and F to provide the main memory chips with the negative logic required to enable one selected chip at a time, while the 2^6 and 2^7 code bits applied to the A6 and A7 inputs address one of four 64-bit sections of the selected memory chip. Dual clocked data-type flip-flop latch U43 transfers the two channel-select LSB's applied to data inputs D1 and D2 to outputs Q1 and Q2 on occurrence of the EOC pulse (applied to the CL input, pin 5). Clocking the bits through by the EOC pulse prevents change of memory-channel selection while in mid-scan during periods 1 and 2 of a program cycle. The $\overline{\text{CSE}}$ and $\overline{\text{CSS}}$ inputs from the program sequencer board are combined by NOR gate U7D to produce Chip Enable for the main memory. Since U1 is enabled on logic low, and disabled (all outputs low) on logic high, U8C is employed to invert the chip enable signal as required for properly operating U1. The power fail latch output of the program sequencer board is applied to the inhibit inputs of U1 and U7B, pins 11 and 5 respectively. Power fail logic high inhibits main and interrupt memory chip enable signals, as discussed in the program sequencer description above. $\overline{\text{CSI}}$ received on board pin C6 from the program sequencer board, is inverted by power-fail inhibit latch U7B and applied to the strobe input of the interrupt

memory (U2) to serve as the Chip-Enable input. (The specified chip-enable inputs, CE1 and CE2, of the interrupt memory are applied along with the strobe input to an AND gate internal to the chip. Because the CE1 and CE2 inputs are held at constant logic high by the battery, the strobe input alone controls the chip enable function.) Occurrence or non-occurrence of Chip-Enable pulses for main and interrupt memories during periods 1 or 2 of a specific program cycle can be determined by referring to Table 4-7. Chip Enable pulses go high at the beginning of Clock 1 pulses and go low at the beginning of Clock 4 pulses, during indicated periods 1 and/or 2 of the program cycle. Chip Enable is low in periods 3 and 4 for all major mode and sub-mode cycles, as may be ascertained from the basic timing diagram, Figure 4-27.

The X1 and X2 inputs received on board pins C4 and C5, respectively, from the program sequencer board, are combined with Clock 2, received on board pin B14 from the program sequencer board, by NAND gates U9D and U9C to produce inverted write enable pulses for the main and interrupt memories. The U9D output is applied directly to the interrupt memory, since U2 requires an inverted write-enable logic input. U16B inverts the U9C output so that non-inverted write-enable pulses are applied to the main memories. Occurrence or non-occurrence of Write Enable for main and interrupt memories during periods 1 and 2 of a specific program cycle can be determined by referring to Table 4-7. Write Enable pulses occur simultaneously with Clock 2 pulses in periods 1 and/or 2 when active, and are inhibited during periods 3 and 4 for all major mode and sub-mode cycles.

Board input X1 is high only during program cycle periods in which Write Enable Interrupt occurs, and board input X2 is high only during periods in which Write Enable Main occurs (Table 4-7). These two inputs are combined by NOR gate U7A, and the NOR output is inverted by U8D to result in an overall OR function. The OR input to U9A permits data to be applied to the memories only during periods in which Write Enable occurs. When power fails the output of U7A goes high, while an internal diode at the input of U8D provides a low impedance path to ground to protect the CMOS input. Diode CR1, situated between U7A and U8D, becomes reverse biased on power failure, thereby preventing drain on the battery by U8D (U7A is powered by the battery, which is not necessary for this part of the circuit. However, U7A is on the same chip as U7B, which must remain active when power fails.) In normal operation resistor R3 provides a forward-bias current path for CR1 on logic low, and performs a hold-up function on logic high, such that CR1 becomes reverse-biased and +5 V is applied to U8D via R3.

Shift Register. - The front panel shift register is composed of integrated-circuit shift registers U17 through U24 connected in tandem. Clock 2, received on board pin B14, is applied directly to the clock input of U17, and is inverted by U16A for application to U18 through U24. U17 clocks on the downward (trailing edge) transistions of the clock pulses, and inversion provided by U16A causes the remaining (positive-edge triggered) stages to also clock on the trailing edges of the clock pulses. Both the receiver register and front panel register are clocked on the trailing edges of Clock 2, which is done to permit

the memory write function to occur (on leading edges of Clock 2) before the memory input data from a shift register changes.

Data from the data node is clocked into the front panel register during period 2 of the program cycle. The data node input is applied to pin 1 of U17, and the bits of the data word are transmitted down the 64-bit shift register until the first bit is loaded into the last stage of register U24. When the register is fully loaded the clock is stopped (see timing diagram) and the first (unused bit 1 - logic low) bit output from pin 13 of U24 is applied to the multiplexer via board pin A13. We may also note the locations of the other bits of the data word: The second bit labled "AGC DUMP" on the schematic can be high only if shifted in from the computer while in the remote mode. The tuned frequency data located in U21, U22, U23, and two stages of U24 is applied to the tuned frequency display. The display has built-in storage and is updated by the EOC pulse in period 3. Shift register section U20 contains the detection mode, IF bandwidth, and gain mode data words. These outputs are applied to the switch encoder board (which is updated in period 3 by EOC and load C). U18 and U19 contain the BFO frequency data word, and 16-stage static shift register U17 provides storage space for the signal level and rf gain data and two spare bits. Note that the spare bit shown on the data word diagram (in Section 3 of this manual) as separating the detection mode and BFO frequency data, is at this point located in stage 8 of U19, while the BFO frequency MSB is in stage 1 of U19, and these locations do not correspond to the parallel load BFO data designations. It may also be noted that the parallel load inputs to shift register stages U20 through U24 are likewise offset by one bit. This offset will be resolved during a synchronous loading operation at the beginning of period 1 of the next program cycle, when the clock becomes active again.

At the beginning of period 1, inverted Load A received on board pin 13 is inverted by U37A and applied to the parallel entry (PE) command inputs of shift register sections U20 through U24. Note that Load A is received only when in the local mode or memory write sub-mode (see Table 4-7). The register sections are operated in the synchronous mode, such that they parallel load data on the positive transistion of their clock (CL) inputs (trailing edge of the first clock 2 pulse) while the Load A command applied to the parallel entry inputs is high. Since the data word must move ahead one bit on the first clock 2 pulse, it is necessary to load the parallel data into the register one bit ahead of the positions occupied by the corresponding bits of the data word before the first Clock 1 pulse occurred; hence the 1 bit offset in the parallel input data lines. The parallel data applied to U20 through U24 is explained further below.

Similarly, shift register sections U18 and U19 may or may not be loaded synchronously at the beginning of period 1, depending on whether or not U15A permits Load A to pass through NAND gate U10C. If U15A (which will be discussed in detail below) does not permit U10C to pass Load A, the parallel data inputs of U18 and U19 are not enabled and the data is moved ahead one bit on the first Clock 2 pulse by normal shift register action. If Load A is gated through U10C, however, the parallel data inputs are enabled and the parallel BFO frequency data is synchronously loaded into the shift register, with a 1 bit offset, on the first Clock 2 pulse. Note that when load A commands parallel entry, the

first bit stored in U17 (spare bit preceeding RF gain MSB - see data word) must be parallel loaded into position 1 of U18 because U18 does not accept serial data when it is operating in the synchronous parallel enter mode.

The data stored in U17 serially moves ahead 1 bit when the first Clock 2 pulse occurs, as this shift register section only provides storage for rf gain and signal level data, and no parallel entry function is performed. When the Load A command is removed from shift register sections U18 through U24, they revert to the normal serial mode, and the next 63 period-1 Clock 2 pulses serially shift the data word out of the register to the multiplexer (on the receiver register board), via board pin A13.

BFO Frequency A/D Converter. - The principle function of this circuit is to convert the analog voltage from the front panel VAR BFO potentiometer to digital form suitable for loading into the front panel shift register. The front panel BFO potentiometer input received on board pin C11 controls the output pulse width of one-shot MV-operated timer U14. The pulses from U14 are inverted by U16F and applied to NOR gate U10B. The duration of each pulse determines the number of 250 kHz system-clock pulses (received on board pin B12 from the synthesizer section) gated through U10B for application to the clock input of the binary counter composed of tandem-connected counters U11, U12, and U13. Eleven counter stages fix the maximum count at 2047, which is more than sufficient to provide the receiver BFO with the required tuning range and resolution. One-shot MV U14 is triggered at the beginning of each period 1 by the low transistion of the inverted Load A command applied to trigger-input pin 2. To avoid clocking the binary counter while the receiver register is updating (on first Clock 2 pulse), the Load A output of inverter U37A disables U10B for the duration of the Load A command, thus delaying application of clock pulses to the counter. The count stops at the trailing edge of the U14 gate pulse, and the resultant eleven-bit binary code from the counter is parallel loaded into the receiver register on the first Clock 2 pulse of the next period 1 (if Load A passes through U10C - see discussion below). The first Clock 3 pulse of each period 1 is gated through NAND gate U38A by the Load A command, to reset the counter immediately after the receiver register is loaded with the count from the preceeding program cycle, thus permitting the next count to start from zero when initiated by the trailing edge of the Load A command.

On the occurrence of each EOC pulse, clocked data-type latches on the switch encoder board are updated with the outputs from U20 of the receiver register. The stored detection mode word is returned (middle bit inverted) to this board, via board pins B13, C1, and C2, for combination by NOR gate U10A. As may be ascertained by referring to the detection mode code on the data word diagram in Section 3 of this manual, the output of NOR gate U10A is high only when the receiver's detection mode is CW FIXED. The output of U10A is inverted by U16E for application to the parallel entry command inputs of the BFO A/D converter counter such that the counter loads a BFO frequency code of 00000000000 (parallel inputs tied to ground externally to the board) when in the CW fixed detection mode, but operates in the counting mode for all other detection modes. The CW FIXED logic high output from U10A is also applied to the reset input of

data-type flip-flop MV U15A, forcing the Q output low to enable NAND gate U10C, which in turn permits the Load A command to be applied to the parallel entry inputs of U18 and U19. Therefore, in the CW FIXED detection mode, the receiver updates with a BFO frequency code of 00000000000.

For detection modes other than CW FIXED, the output of U10A is low, which permits the BFO frequency A/D converter counter to count clock pulses and permits data-type flip-flop U15A to operate normally. The Lock signal received on board pin C3 and applied to the data input (pin 9) of U15A is clocked through to the Q output (pin 13) on the positive-going transistion of the Load A command applied to the clock input (pin 11), thus permitting the Lock signal (generated on the switch encoder board) to determine whether or not the BFO frequency A/D converter output is loaded into the front panel register at the beginning of period 1 of a program cycle in which Load A occurs. As will be discussed in the switch encoder board description, when not in the CW VAR detection mode the Lock line is high and prevents parallel loading of U18 and U19, except when in the CW FIXED mode in which the output of U15A is forced low by the reset input. In the CW VAR mode, the Lock line goes low the first time the CW VAR button is pressed so that the BFO frequency may be adjusted, and the Lock line returns to high the second time the CW VAR button is pressed to effectively lock the BFO to the frequency set. Also, on return to the local mode after a memory execute sub-mode, if the data word called up from memory indicates the CW VAR mode, the Lock line will initially be high.

Manual Tuning Up/Down Counter. - The manual tuning up/down counter comprises presettable up/down counter decades U25 through U31. The tuning-dial sense-circuit (to be described below) clock output, the frequency of which is proportional to the rate of rotation of the tuning dial, is applied in parallel to the clock inputs of the counter decades (pin 15 of each decade), and the up/down steering line from the tuning dial sense circuit is applied in parallel to the up/down inputs of the counter decades (pin 10 of each decade). When the tuning dial is rotated in the clockwise direction the up/down line goes high and the counter counts up in 10 Hz steps, one for each clock pulse. The up/down line goes low and the counter counts down in 10 Hz steps when the tuning dial is rotated in the counterclockwise direction. Each decade counts from 0 through 9 or 9 through 0 on positive clock transistions, returning to 0 on each 10th count counting up, or returning to 9 counting down. Decade counting is achieved by the connection of the carry output (CO) of each stage to the carry input (CI) of the following stage. Carry out (logic low) appears on the count of 9 when counting up, or appears on 0 when counting down, provided the carry in from the preceeding stage is low. The carry output performs a clock enable function internally to the stage to which it is applied, such that the count can be advanced (in either direction as determined by the up/down line) by the clock pulse only if the carry from the preceeding stage is present. That is, if a stage generates a carry out on the count of 9 (counting up) or 0 (counting down), on the next clock pulse the stage to which the carry is applied will advance up or down one count, then remain disabled until another carry is received. The BCD output, representing frequencies from 500 kHz to 30.5 MHz as limited by the end-point

recognition circuit described below, is available from the Q outputs of the overall-counter decades.

When the receiver is in the local operating mode or in the memory write sub mode, Load A causes the count accumulated in the counter (Q outputs) to be parallel loaded into the receiver register (D inputs of U21 through U24) on the first Clock 2 pulse of period 1 (see front panel register description above). In other modes Load A does not occur and the counter output is npt loaded into the receiver register. However, in returning to the local mode from another mode, a parallel load operation prevents the receiver frequency from changing from that programmed in the previous mode, until the operator deliberately changes it by turning the tuning dial. In period 3 of the local/remote return sub-mode, an inverted Load C pulse, received on board pin BN, is inverted by U16D and U38C (pin 9 of NAND gate U38C is normally high) for applicati to the parallel entry command inputs (pin 1) of the up/down counter decades. This parallel loads the tuned frequency data word presently in the front panel register (Q outputs of U21 through U24) (clocked in from the receiver register during period 2 of the program cycle) into the parallel data (J) inputs of the up/down counter. The up/down counter starting-point frequency is thus the most recent frequency to which the receiver was tuned in the preceeding operating mode. Pins 5 and 12 (C2 and C4 inputs) of quad multiplexer switch U32 are normally high and route the 10^7-decade data shift register outputs (I2 and I4 of U32) to the 10^7 -decade up/down counter stage (J1 and J2 inputs of U31) for parallel loading as required.

End-Point Recognition Circuit. - The end-point recognition circuit comprises quad multiplexer switch U32, logic gates U38C, U39 A, B, and C, U40 A, B, and C, U41 B and C, NOR latch U41 A and D, inverter U37C, and two one-shot multivibrators composed of U38B, U37E, CR7, R23, and C2 and U38D, U37B, CR6, R20, and C3. When the counter output frequency lies betwe 00.50000 MHz and 30.49999 MHz, inclusive, the outputs of U41C and U37C are low, which results in a logic high output from U41B. Also, in the quiescent state, capacitors C2 and C3 of the respective one-shot MV circuits are fully discharged, such that the inputs of inverters U37E and U37B are at logic low, and the corresponding outputs are at logic high. The logic high quiescent-state output of U37B and the logic high in-range output of U41B produce a logic low output from U38D. The logic low from U38D, applied to gating inputs C1 and C3 of quad multiplexer switch U32, disables the I1 and I3 signal inputs, and the logic high from U37B, applied to gating inputs C2 and C4, gates the two 10 decade bits (I2 and I4) of the tuned frequency data word (from U24) through to the parallel inputs of up/down counter decade U31. The quiescent-state high output of U37E enables U38C so that Load C is permitted to cause U32 to load the two parallel data bits from U24 as previously described. NOR latch U41 A and D can be in either state when the up/down counter is in range.

If the operator rotates the tuning dial such that the count accumulated in the up/down counter reaches the high-end limit of 30.50000 MHz, all of the inputs to U39 A and B go high, which results in a high output from U41C. This hi causes pin 3 of U41A to latch at logic low (if not already in that state), and causes

the output of U41B to go low, which in turn causes the outputs of U38 B and D to go high. The high output of U38D, applied to gate inputs C1 and C3 of U32, gates through the logic low output from the NOR latch. The logic high transitions from U38B and U38D are applied to RC differentiators C2-R23 and C3-R20, respectively, which convert the positive-step transitions to positive spikes. The spikes applied to U37E and U37B cause the outputs of these inverters to go to logic low for the duration of the charge times of C2 and C3, then return to logic high. The logic low pulse outputs are returned to the U38 B and D inputs to produce regenerative feedback which speeds up the low transitions of the pulses. The logic low pulse from U37E is inverted by NAND gate U38C (Load C is normally high) and causes U31 to parallel-load the two logic low bits gated through U32 from U41A. The logic high from U38D, applied to gate inputs C1 and C3 of U32, inhibits the I2 and I4 inputs while the two logic low bits are being loaded into U31. The counter output, therefore, upon reaching the upper limit of 30.5 MHz, immediately is reset to 00.5 MHz. Immediately upon reset of the counter, the output of U41C goes low, causing the output of U41B yo go high. This high transition causes the outputs of U38B and U38D to go low, which in turn causes the respective differentiator circuits to tend to produce negative spikes. CR6 and CR7 clip the negative spikes to protect the inputs of U37 E and B. The logic low output of U38D which occurs as soon as counter stage U31 is loaded causes multiplexer switch U32 to revert to the former quiescent condition. If the operator continues turning the tuning dial clockwise, the count will continue to increase but from the lower limit frequency to which the counter was reset.

If the operator rotates the tuning dial such that the count accumulated in the up/down counter reaches the low-end limit of 00.49999 MHz, all of the inputs of U40A, B and C go to logic low, which results in the output of U37C going high. The logic high from U37C sets up latch U41 A and D such that pin 3 of U41A latches at logic high, and causes the output of U41B to go low. The remaining action is identical to that described in the preceeding paragraph, except that two logic high bits are parallel-loaded into U31 instead of two logic low bits, as determined by the state of latch U41 A and D. The counter is thereby reset to a count of 30.4999 MHz, which immediately causes the end-point recognition circuit to revert to its former quiescent condition. If the operator continues to turn the tuning dial counterclockwise, the count will continue decreasing but from the upper limit frequency to which the counter was reset.

Tuning Dial Sense Circuit. - The tuning-dial sense-circuit schematic is located on the lower portion of sheet 1 of the front panel register schematic. This circuit provides clock and up/down steering lines to the up/down counter described in the preceeding paragraphs. The output clock rate is non-linearly proportional to the rate of rotation of the tuning dial, as described in the operating instructions in section III of this manual, and the logic level of the up/down line is a function of the direction of rotation of the tuning dial.

The tuning dial sense circuit receives two inputs (board pins C14 and CR) from two photodiodes in the tuning dial encoder assembly. As will be discussed in the schematic description for that assembly, these two signals are square waves of frequency proportional to the rate of rotation of the tuning dial,

and are identical except for a ± 90° phase relationship dependent upon the direction of rotation. Inverters U24D-U36F and U42C-U36B are connected in regenerative feedback configurations which causes these circuits to perform similarly to schmitt triggers. These circuits reduce the rise and fall times of the leading and trailing edges of the squarewaves received from the tuning dial encoder assembly, necessary to meet clock input requirements of edge-triggered data-type flip-flop MV's U34A and U34B, particularly at low tuning-dial rotation rates for which the photodiode-output rise and fall times are longest.

The shaped "clock" squarewave is applied to the clock inputs of flip-flop MV's U34A and U34B, and the shaped "direction" squarewave is applied to the data input of U34A. Taking the "clock" squarewave as reference, if the tuning dial is rotated in the clockwise direction, the "direction" squarewave lags the "clock" squarewave by 90 degrees, such that the data input of U34A is low every time a clock input high transition occurs. This low is clocked through U34A, and the output of U34A stays low until the direction of rotation is reversed. Similarly, if the tuning dial is rotated in the counterclockwise direction, the "direction" squarewave leads the "clock" squarewave by 90 degrees, such that the data input of U34A is high every time a clock input high transition occurs. The logic high is clocked through U34A, and the output of U34A stays high until the direction of rotation is reversed. The output of U34A is inverted by U36A for application to the up/down counter. An input (external sense) received on board pin CM from an optional control box (via filter A24) external to the receiver may control the up/down line. The junction of R31 and R12 performs a wired-OR function for the two control sources.

The clock generator circuit utilizes an averaging circuit that requires constant-width input pulses, one for each logic high transition of the tuning dial encoder assembly "clock" output squarewave. Data-type flip-flop U34B is connected in a one-shot MV configuration to serve this purpose. Assume an initial quiescent condition in which the Q output of U34B is low, in which case C8 is fully discharged and the reset (R) input is low. Upon reception of a high transition on the clock (C) input, from the clock shaping circuit, the +5 V supply voltage (VDD1) on the data (D) input is clocked through, and the Q output goes high. CR5 is reverse-biased and C8 begins to charge slowly through R10. When the charge on C8 reaches the minimum TTL logic high level, approximately 2 volts, the Q output of U34B is reset to logic low. CR5 now is forward biased and quickly discharges C8, thus returning the circuit to the former quiescent condition. The low-going pulses from the complementary $\overline{Q}$ output are inverted by U36D for application to the averaging circuit.

The averaging circuit is composed of averaging components C5, R27, CR4, R16, and C11, and quick-stop discharge components CR3, C4, R14, and Q1. Emitter-follower Q2 is the averaging-circuit output buffer. With no pulses received from U36D, the voltage at the base of Q1 is 0 V. The dc current path through R27 and CR4 tends to charge C11 toward the positive voltage at the junction of R16 and R17; however, Q1 becomes forward biased and clamps the C11 voltage to one emitter-junction drop of 0.6 V. The output voltage of emitter-follower Q2 is therefore 0 V, due to its emitter-junction voltage drop. A positive pulse output from U36D is coupled to the base of Q1 by CR3, reverse-biasing Q1 and

charging C4 to the peak pulse level (less one diode drop). The pulse also is coupled to the cathode of CR4 so that CR4 becomes reverse-biased when the pulse voltage exceeds the voltage at the junction of R16 and R17. (R17 adjusts the CR4 clamp voltage for stable operation of the circuit.) C5 charges, and C11 charges to a higher level, through R27 at a rate determined by the value of R27 and the peak pulse voltage. Since the pulse is short, C11 does not charge to the peak pulse level. On the trailing edge of the pulse CR3 becomes reverse biased and C4 starts to discharge through R14. The voltage developed across R14 keeps Q1 reverse biased for a short period. Also, CR4 becomes forward biased and quickly discharges C5. However, the discharge rate of C11 is limited by the value of R27, and if additional pulses are received before C4 discharges to the point where Q1 again becomes forward biased, the voltage on C11 will be proportional to the average pulse rate (and therefore the tuning dial rotational rate). If the operator stops turning the tuning dial so that no more pulses are generated, after a short time C4 will be discharged to the point where Q1 again becomes forward biased, quickly discharging C11 to return the circuit to the quiescent condition. This quick-discharge feature prevents overshoot in case the operator suddenly stops turning the tuning dial.

The averaging circuit output from emitter-follower Q2 is applied to FET transistors Q3 and Q4, which in turn control the frequency of VCO-operated timer U33. C12 is the timing capacitor, and Q3 and Q4 serve as voltage-controlled resistive dividers which are also part of the timing circuit. Q3 and Q4 are operated at the knee of their dynamic operating range, which results in the VCO output frequency being exponentially proportional to the averager output voltage, and, therefore the tuning-dial rate of rotation. Resistor R18 adjusts the operating range of Q3 and Q4. At low tuning-dial rotational rates, the averager output is virtually zero, which in itself, results in little or no output from the VCO. However, the one-shot MV output pulses applied to the averaging circuit are also applied directly to the VCO-operated timer via inverter U36E. These pulses cause U33 to produce one output pulse for each input pulse, which therefore permits high-resolution (10 Hz steps) tuning. At slightly higher rotational rates the averager output takes hold and starts to increase the output frequency of the VCO. At even higher rotational rates the averager output dominates and the VCO frequency is exponentially proportional to the rate of rotation. Rapid band-edge to band-edge tuning is thus easily achieved. The VCO output is applied to the up/down counter clock inputs via parallel-connected (for additional drive) NAND gates U35 A, B, and C. Inverted Load A applied to the enable inputs of the NAND gates prevents the up/down counter from incrementing while the front panel register is updating.

An external tuning control voltage, received on board pin CN from the optional tuning control box via tuning connector filter A24, permits the optional tuning control box to tune the receiver in conjunction with the up/down input from the optional control box described above. The external control voltage is applied to the gates of Q3 and Q4 in parallel with the averager output.

Power-Down Battery. - BT1 is the power-down battery. When the receiver is operating normally, BT1 is kept fully charged to +5 V via diode CR2. When power fails, the +5 V regulated supply voltage drops to zero, and CR2

becomes reverse-biased to keep BT1 from discharging through receiver circuitry not meant to be supplied by the battery. The battery voltage is applied to the memories and associated gates on this board and to the interrupt circuit on the program sequencer board.

4.5.2.3 Type 791137 Switch Encoder Board (A21). - This board contains the front panel pushbuttons, pushbutton lighting circuits, and logic circuitry related to pushbutton and lighting circuitry operation. Figure 7-23 is the schematic diagram for A21.

Pushbutton Circuitry and NAND Latches. - The left half of the schematic shows the detection mode, gain mode, and IF bandwidth-select pushbuttons (except CW VAR button - shown at lower right), pushbutton coding gates (diode arrays), and eight NAND latches which store the selections made by these pushbuttons or made automatically by inputs from the front panel register. NAND latches U8 A and C, U13 C and A, and U13B-U9B store the detection mode code, NAND latches U9 C and A and U10 B and A store the gain mode code, and NAND latches U12A-U10C, U11 C and B and U12B-U11A store the IF bandwidth code. These logic codes are routed to the front panel register board for loading into the front panel register at the beginning of period 1 (in local mode only) of the program cycle, as explained in the description of the schematic and in the functional block and timing diagram descriptions.

Since Load C occurs for local-return sub-mode cycles only, assume for the time being that the unit is in the normal local operating mode, in which case the $\overline{\text{Load C}}$ board input (pin 5) is high. This input is inverted by U17A, so that NAND gates U2 A and B, U4 C and C, U5 A, B, C, and D, U6 A, B, C, and D, and U7 A, B, C, and D are disabled. With these NAND gates disabled, the detection mode, gain mode , and IF bandwidth shift-register outputs, received on board pins 16, 13, U, 17, F, 6, E, and 4, cannot control the states of the NAND latches. The outputs of the disabled NAND gates are logic high, which therefore permits the outputs of the pushbutton diode-logic arrays to control the NAND latches.

The diode-logic arrays are connected in OR configurations which route the pushbutton momentary outputs to appropriate NAND latch inputs. With no pushbutton pressed, +5 V supply voltage is applied to the NAND latch inputs via resistors R2 through R18, holding the respective latch inputs at logic high. The latches therefore remain in the states set up by previous pushbutton or automatic control (Automatic preset of the latches in period 3 of a local/remote return sub-mode cycle is described below). If a button is pressed, pull-down logic low (assume for the present that the outputs of U22D and U22F are low) is coupled by diodes to the two or three latches which produce code bits corresponding to the function being selected. The pushbutton sets up the latches for high or low outputs, depending on the latch inputs to which the pushbutton outputs are applied. The diodes connected between these same latch inputs and other pushbuttons become reverse biased to prevent the logic low from being applied to other latch inputs.

Diodes CR26, CR27, and CR28 couple the ISB, LSB, and USB detection mode pushbutton outputs to the "position 5" (8 kHz) IF bandwidth pushbutton circuit, so that when the operator selects ISB, LSB, or USB, the 8 kHz bandwidth is automatically selected. NAND gates U2C and U2D decode the detection mode code such that the output of inverter U22D is high for ISB, LSB, and USB detection modes, and low for all other modes. The logic high disables all IF bandwidth pushbuttons except the 8 kHz button, thereby preventing selection of other bandwidths when ISB, LSB, or USB detection mode is selected. (The respective detectors in the receiver section require the wider IF bandwidth for these detection modes.)

Diode CR29 couples the ISB detection mode pushbutton output to the normal AGC (NAGC) pushbutton circuit, so that normal AGC is selected when the ISB detection mode is selected. This is done because the ISB demodulators require that the receiver section be operated in the normal AGC mode to provide proper output. NAND gate U12C detects when the receiver is in the ISB mode, and disables the hold AGC (HAGC) button by providing logic high via inverter U22F. The manual gain mode button (MAN) is not disabled, however. The latch which provides the inputs to U12C (U23) is described below.

As discussed above in the functional block diagram description, if the unit is returning to local from power failure or another mode, it is necessary to preset the NAND latches. Therefore, the unit goes through a return sub-mode cycle before returning to local, in which Load C occurs (see timing diagram) at the beginning of period 3 of the program cycle. Load C (output of U17A) enables gating NAND latches U2 A and B, U4 C and D, U5 A, B, C, and D, U6 A, B, C, and D, and U7 A, B, C, and D, permitting the detection mode, gain mode, and IF bandwidth codes, received from the shift register on the receiver register board via board pins 16, 13, U, 17, R, 6, E, and 4, to set up the NAND latches with the codes on the data word. The codes stored in the latches are returned to the receiver register for loading at the beginning of period 1 of the next program cycle. These NAND gates are disabled at all other times.

Pushbutton Lighting Circuits. - The detection mode, gain mode, and IF bandwidth codes from the receiver shift register are loaded into data-type clocked storage latches U23 and U24 by the $\overline{EOC}$ pulse (received on board pin 19 and applied to clock input pin 5 of each latch) during period 3 of each program cycle. The inverted or non-inverted ($\overline{Q}$ or Q) latch outputs are buffered (and inverted if necessary), then applied to BCD-decimal decoders U20 and U21 and decoding NAND gates U18 C and D and U19A, which outputs in turn illuminate the pushbuttons corresponding to the detection mode, gain mode, and IF bandwidth indicated by the data word. Stored detection mode outputs are also applied via board bins X, H, and K to the BFO A/D converter circuit on the front panel register board, for use as discussed in the schematic description for that board.

The inhibit input of the detection mode decoder, U20, is operated by NOR gate U14A. The NOR gate output goes high to inhibit U20 only when all four inputs go low. This inhibit feature is used to flash the CW VAR light when the VAR BFO control is active while in the variable cw detection mode. The output of low-frequency-connected-oscillator timer U15 is connected to one input of the

NOR gate, to flash the light when the other inputs are low. Since the VAR BFO control is active only while the unit is in the local mode or memory write sub-mode, one of the NOR gate inputs must go low when the unit goes to the local mode. U3A performs this function by decoding the two most significant mode code bits, received on board pins 9 and J from the program sequencer board. NOR gate U14B and inverter U22E provide a logic low input to U14A when the data word indicates that the variable cw detection mode is in effect.

The output of data-type flip-flop U1 provides the remaining input to U14A. U1 and U14B also produce the board lock output (pin W), thus coordinating the flashing of the BFO VAR button with the loading of the BFO frequency code into the front panel shift register. When the unit is not in the variable BFO detection mode, the logic high output from U22E holds U1 in the reset condition, such that the $\overline{Q}$ output holds at logic high. This logic high prevents the BFO frequency A/D converter output from being loaded into the front panel shift register (except while in the fixed BFO detection mode), as covered in the schematic description for the front panel register board. When in the variable BFO detection mode, the logic low output of U22E permits the board Lock output and the flashing of the CW VAR button to be controlled by the CW VAR button via NAND latch U3 C and D and U1. The NAND latch eliminates the effects of button bounce, and U1 functions as a 2:1 divider. Upon the establishment of the variable cw detection mode, the $\overline{Q}$ (lock) output of U1 is initially high, so that the button light is steady and BFO A/D converter data is prevented from being loaded into the front panel register. The output of U1 goes low the first time the CW VAR button is pressed so that the button light flashes and BFO A/D converter data is permitted to load into the front panel register (at the beginning of period 1 as commanded by Load A). The output goes high again the second time the button is pressed, restoring the initial conditions.

Note that the input on board pin V, received from the execute circuit on the program sequencer board, is normally low. This output goes high only for memory execute sub-mode program cycles, ensuring that U1 is reset to the lock condition ($\overline{Q}$ output high) as an initial condition upon reverting to the local mode from a memory execute sub-mode. (The unit automatically goes through a local/remote return sub-mode cycle after a memory execute sub-mode cycle, then reverts to the major local operating mode.) If while in the local operating mode, a detection mode other than variable BFO is in effect, and the variable BFO mode is selected by pressing the CW VAR button, U1 will initially be in the lock condition by virtue of the previous preset output of U14B. Note that the detection mode code selected from the front panel must be loaded into the front panel register, clocked to the receiver register, and then returned to the front panel register and clocked into storage latch U23 before the output of U14B can change to permit U1 to be operated by the CW VAR button. This delay ensures that the selection of CW VAR by pressing the button does not change the state of U1 to interfere with the establishment of BFO lock as the initial condition.

If in the remote mode the data word indicates the variable BFO detection mode, so that the CW VAR button illuminates, if the operator presses the CW VAR button once (or an odd number of times), the button light will remain steady and the front panel register will not load BFO A/D converter output data (because

Load A does not occur). However, upon return to the local operating mode, the initial conditon will be unlocked variable BFO, with the button light flashing (unless the button was pressed an even number of times while still in remote).

The two most significant bits of the mode code received on board pins 9 and J operate the REMOTE, LOCAL, and MEMORY button lights via U19 B, C, and D, U17 B, C, and F, and decoding NAND gate U3A. The output of low-frequency oscillator U15 is applied to one input of U19D to cause the MEMORY button to flash when in the memory operating mode. (Flashing of the MEMORY button is a reminder to the operator that the frequency displayed may not represent the actual tuned frequency of the receiver.) The output of U3A, which is logic low for the local operating mode, was already discussed above in relation to the input of U14A. This output also functions to enable the ENTER button while in the local mode. The ENTER button output is applied to the corresponding circuit on the program sequencer board. While in the local mode, before the ENTER button is pressed the input on board pin 3, from the program sequencer board, is at logic low. The first time the ENTER button is pressed, the input on board pin 3 goes high, causing lamp drivers Q1 and Q2 to light the ENTER button lamp. The second time the button is pressed the input goes low again and the light extinguishes (at the same time the memory write sub-mode is executed).

The LOCAL, REMOTE, MEMORY, and EXECUTE pushbuttons operate in conjunction with the mode code circuitry on the program sequencer board. The LOCAL button provides logic low when pressed, while the remaining three provide open circuits which permit pull-up resistors on the program sequencer board to produce logic highs. The EXECUTE button also provides a ground which causes the button light to illuminate when pressed.

The SIGNAL STRENGTH and LINE AUDIO buttons operate NAND latch U18 A and B, which in turn drives corresponding button lights and provides a select logic output (board pin 22) to the meter circuit in the receiver section (boards A13 and A14). The NAND latch permits the most recently pressed button to illuminate, while the other remains extinguished. The button light illuminates when the corresponding latch output is logic low. Diodes CR53 and CR54 prevent the light supply voltage from being applied to the +5 V NAND inputs when the respective latch outputs are at high-impedance logic high (for which the lights are off). In this case an open input circuit serves as logic high.

Transistor Q3 is an emitter follower which converts the +10 V supply voltage to a lower volage for supplying the button lights. The setting of variable resistor R25 determines the exact lamp supply voltage, thereby controlling the lamp intensity. A logic low output from any of the lamp drivers causes the lamp to illuminate, while on logic high the driver presents a high impedance so that insufficient current flows to illuminate the lamp.

4.5.2.4 Type 791140 Receiver Register Board (A17). - Refer to the schematic, Figure 7-19. The receiver register board contains the receiver shift register, storage registers for storing shift register output data, logic decoders, a signal strength A/D converter, an rf gain A/D-D/A converter, a preselector range decoding circuit, and the data multiplexer. These circuit sections are shown on the simplified block diagram, and are touched on briefly in the block diagram description.

Multiplexer. - Quad switch U38 is the main data multiplexer for the digital control section. Multiplexer inputs VI-1 through VI-4 receive the remote data word from the I/O module (via board pin B20), the front panel and memory data words from the front panel register board (via board pins B7 and B8, respectively), and the receiver register data word output from pin 2 of U7 on this board ("A" input), respectively. The four outputs of U38 (VD-1 through VD-4) are connected together to form the common data node. The data node is connected to U32 on this board, which is the first stage of the receiver shift register, and to the I/O module and the front panel register boards via board pin C4. Data word routing is described fully in the functional block diagram description and need not be mentioned further here. The binary-coded multiplexer address inputs received on board pins AA and BH, from the program sequencer board, are decoded by NOR gates U37 A through D and inverters U45E and U45F. The decoder outputs are applied to the quad switch channel-select inputs; logic high is the select level. Refer to Table 4-7 for the multiplexer address code.

Receiver Shift Register. - The receiver register is composed of tandem-connected shift register sections U32 and U1 through U7. The shift register sections are parallel-clocked by the Clock 2 pulses received on board pin C3 from the program sequencer board. Clocking occurs on the trailing edges of the Clock 2 pulses, to permit time for the completion of the memory write function (on leading edges of Clock 2) before the data from the receiver shift register changes. The serial data word is clocked into the receiver shift register during period 1, and clocked out again in period 2. Data clocked in during period 2 is clocked out again during the next period 1 and not used. 64 period-1 clock 2 pulses clock the data bits through U32 (in pin 1, out pin 3), through U1 (in pin 10, out pin 1), then through the six identical tandem-connected stages U2 through U7 (in pin 7, out pin 2 of each shift register stage). After the completion of the last Clock 2 pulse of period 1, the data word is fully loaded into the shift register chain, with the first bit (unused bit - logic low) applied to the multiplexer from the output of U7 (pin 2 of U7 connected to pin 8 of U38), and with the data bits in U2 through U7 applied via the parallel (Q) outputs to storage register (U8 through U19) inputs corresponding to these bits. The locations of the various data bits in these shift register sections may be ascertained by referring to the corresponding storage register output designations on the schematic. Also, the signal strength data bits are located in U32, and the rf gain data bits are located in U1. U32 and U1 are 8-bit shift registers; however, only seven parallel-output (PI2 through PI8) lines are connected to U32, and only seven parallel input (A2 through A8; A1 is fixed at logic low) and seven parallel output (B1 through B7) lines are shown connected between the A/D-D/A converter and U1. The unused bits of these shift registers are the two spare bits shown on the data word diagram as preceeding the most significant bits of the rf gain and signal level data words. Note that at this point that the seven bits in U1 are properly positioned with respect to the seven parallel output lines, ready for parallel loading into binary counters U20 and U21 of the D/A-A/D converter (only if in the remote operating mode); however, these bits and the seven bits in U32 are not yet properly positioned with respect to the parallel-load input lines. This off-

set is required for a synchronous load operation explained below. (The A/D and A/D-D/A converters to which these lines are connected are described below.)

Load B received on board pin AB is inverted by U45D to produce Load B for executing shift register and storage register load operations at or near the beginning of period 2. Load B also controls the signal strength and rf gain A/D converters. Although these converters will be described completely below, it is appropriate at this point to mention that if in the remote operating mode, at the beginning of period 2 the leading edge of Load B causes binary counters U20 and U21 to parallel-load the rf-gain data word from U1 (in other modes this load operation does not occur). Storage registers U8, U9, and U10 load on the low-going transitions of their clock (pin 10) inputs, making it necessary for Load B to be inverted by U28C so that these storage registers are updated at the beginning of period 2 by the leading edge of Load B. The most significant bit of the detection-mode code is applied, via U26B, to the word select inputs of the BFO frequency storage registers. If the MSB is logic low (AM, FM, BFO fixed, BFO variable), the storage registers load Word 1 (BFO data from the shift register); if the detection-mode code MSB is logic high (ISB, LSB, USB, AM-NL), the storage registers load data Word 2 (A2 through D2 inputs of each register), which is fixed for all bits except bit 12 (X10000000000 - with the "X" indicating bit 12, which is obtained from the shift register and is the spare bit shown preceeding the BFO-frequency MSB on the data word diagram).

C16, R15, CR5, and U24C comprise a one-shot multivibrator circuit which produces a low-going 5 μs pulse in response to the low-going leading edge transition of the Load B outut of U28C. This pulse is applied to the load command clock inputs (pin 5 or 8) of storage registers U11 through U19. These registers, which load on the high transitions of their clock inputs, therefore update with data from the shift register approximately 5 μs after the beginning of period 2 of the program cycle. This delay prevents detection mode code storage register U11 from updating until after the BFO storage register (U8, U9, and U10) word selection has stabilized, and also prevents the trailing edge of the last Clock 4 pulse (received on board pin A5 and applied to U41 and U42) of period 1 from updating the preselector range decoding circuit while the storage registers are updating. (The preselector range decoding circuit, comprising U41 and U44, is described fully below.)

When Load B goes high at the beginning of period 2, shift register stages U32 and U1 change from serial to parallel operating modes. The first Clock 2 pulse of period 2 therefore shifts all bits in the overall shift register one position except the signal strength and rf gain bits in U32 and U1. This results in logic low being clocked into the first position of shift register stage U2, which ensures that the unused bit preceeding the rf gain MSB is logic low. Shifting the data word forward one bit causes the active output bit to be replaced by bit 2 as should occur as part of normal shift register operation. The first Clock 2 pulse of period 2 also causes U32 and U1 to synchronously parallel-load the respective A/D converter outputs. The parallel data is loaded one bit ahead of the formerly-mentioned fully-loaded positions, since the overall data word must advance one bit on occurrence of the first Clock 2 pulse. Note that parallel-input bit 1 of U1 (pin 16) is obtained from NOR gate U22B. Because board pins C6

and C8 are grounded and pin C7 is fixed at logic high, this input is held at logic low by U22B, thus ensuring that the unused bit preceeding the signal level MSB (see data word diagram) is logic low. (The fault output from the 2nd LO/BFO is not used.)

The detection mode, IF frequency, and gain mode binary codes stored in registers U11 and U12 are decoded by decoders U35, U36, and the decoder composed of U23 C and D and U40 A through D, and the decoder outputs are applied to the receiver section. The function-select output level of each decoder section is logic high. Refer to the data word diagram for tables of the binary codes.

Preselector Range Decoding Circuit. - The preselector range decoding circuit is composed of read-only memory (ROM) U43, 5-bit digital comparators U41 and U42, up/down counter U44, and associated components including the AND gate composed of CR6 through CR9 and R16. The two 5-bit comparators are connected in cascade to form an overall 9-bit comparator. This comparator compares the 9 most significant bits of the BCD tuned-frequency select outputs of storage registers U17, U18, and U19 to the binary-coded output of the ROM. The AND gate comprising CR6 through CR9 and the carry output (pin 12) of the up/down counter decode the upper counter limit for application to the comparator's MSB input. Inverters U28 A, B and D at the output of the comparator change the sense of the comparison ($A > B$ becomes $B > A$, $A < B$ becomes $B < A$, and $A = B$ becomes $A \neq B$); however, the method of clocking the counter again reverses the sense of the comparison, as follows:

The up/down counter U and D input lines (pins 5 and 4, respectively) serve both to clock and steer the counter. Clocking occurs on a high transition of either input, while direction of count is determined by which input receives the clocking transition while the other input remains high. These transitions are controlled by the Clock 4 pulses received on board pin A5 and applied to the Enable input (pin 1 of U42) of the comparator. When Clock 4 is high, all three comparator outputs are low, which in turn results in both counter inputs being high. The comparator updates on the low-going transition of the Clock 4 pulse, and also at this time the comparator output is enabled so that the counter U or D line goes low. The counter does not count at this time, however; instead, the count occurs on the high transition of the U or D line when the comparator is disabled on occurrence of the next Clock 4 pulse. This action again reverses the sense of the inequality, as mentioned above. For example, if at the end of a Clock 4 pulse B is greater than A, the counter D input will go low and the U input will remain high. On occurrence of the next Clock 4 pulse the D input will go high again and the counter will count down one count. Similarly, if at the end of a Clock 4 pulse A is greater than or equal to B (the outputs of U28A and U28B are wired-OR connected), the counter's U input will go low and the D input will remain high. On occurrence of the next Clock 4 pulse the U input will go high again and the counter will count up one count.

The counter's three most significant bits are inverted by U4 A, B, and C for application to the receiver preselector circuit via board pins A1, A2, and A3. The binary code output of the up/down counter is therefore the opposite

of the code shown in Table 4-8. That is, the counter's highest count (1111) produces the lowest output code (000), and the counter's lowest count (0000) produces the highest output code (1111). (The LSB output of the counter is applied to the ROM but not to the preselector code output.)

Each binary code output of the counter causes the ROM to produce a BCD output code corresponding to the lower frequency limit shown in Table 4-8 for the three bits of the range represented by the code. As long as the comparator's B input is less than the A input, or as long as the B input is greater than the A input, the counter will continue to count up or down, respectively, on each high transition of the Clock 4 input. When B = A or is less than A but within the range indicated in Table 4-8 for the binary code input to the comparator, the counter counts up one bit, which then causes B to be greater than A. This immediately causes B to again equal or be less than A, so the counter counts up again on occurrence of the positive transition of the next Clock 4 pulses, and the process continues. Because only three of the four counter outputs are used for the preselector code, the constantly changing LSB does not affect the selection of the preselector.

Table 4-8. Preselector Code

Frequency Range, MHz	Binary Code		
	2^2	2^1	2^0
0.5-0.8	0	0	0
0.8-1.2	0	0	1
1.2-2.0	0	1	2
2.0-3.4	0	1	1
3.4-6.0	1	0	0
6.0-10.0	1	0	1
10.0-18.0	1	1	0
18.0-30.0	1	1	1

Signal Strength A/D Converter. - This circuit comprises cascaded binary counters U33 and U34, D/A converter U31, operational amplifier U30A, comparator U39, NOR latch U47C-U47D, NOR gate U22C, differentiator C1-CR1-R1, driver U25C, and inverters U24 A, D, E, and F. The circuit functions as follows:

Inverter U24A inverts the Load B pulse received from U45D, and the inverted Load B pulse is differentiated by C1 and R1. Diode CR1 eliminates the negative differentiator spike. The positive differentiator spike, which occurs on the trailing edge of Load B, is converted to a low-going 5 μs (approximately) pulse by inverters U24 D, E, and F. This relatively short pulse is applied to the reset inputs (pin 13) of cascaded binary counters U33 and U34 to reset the counter outputs to zero. Digital-to-analog converter U31 converts the counter binary zero output to a zero current output, which is in turn converted to 0 V by operational amplifier U30A. The operational amplifier output is applied to the inverting

input of comparator U39. The signal strength voltage, received on board pin C15 from the the receiver section, and applied to the reference input of the comparator, is negative. Therefore, the output of comparator U39 is logic low. This logic low, in being applied to one input of NOR latch U47C-U47D, permits the positive differentiator spike applied to the other latch input to reset the latch output to logic low. This logic low permits NOR gate U22C to pass 250 kHz system clock pulses received on board pin C13 from the synthesizer section. The counter begins counting these clock pulses upon termination of the logic low reset pulse, which occurs approximately 5 μs after the trailing edge of the Load B pulse. As the count increases, the D/A converter analog output current increases, causing the output voltage of U30A to increase in the negative direction.

As the count increases the point will eventually be reached when the negative output voltage of U30A equals (or rather, very slightly exceeds) the negative signal strength input voltage. At this point the output of comparator U39 changes from logic low to logic high, causing the NOR latch to change state. The resulting logic high output from the NOR latch disables NOR gate U22C, thus stopping the counter. Because the counter counted for a period proportional to the signal strength voltage from the receiver section, the counter's binary code output is numerically proportional to this voltage. This data is parallel-loaded into shift register section U32 on the trailing edge of the first Clock 2 pulse of period 2 in the next program cycle, as previously described. Soon after the data is loaded, the trailing edge of Load B again resets the counter and the NOR latch, thus initiating a new counting cycle.

RF Gain A/D-D/A Converter. - The rf gain A/D-D/A converter functions similarly to the A/D converter described in the preceeding paragraphs. The converter is composed of D/A converter U27, tandem-connected binary counters U20 and U21, operational amplifiers U29A, U29B, and U30B, comparator U46, FET switches Q1 and Q2 with switch drivers Q3 and Q4, NOR latch U47A-U47B, NOR gate U22A, NAND gates U23A and U23B, differentiators C1-R1-CR1 and C2-R2-CR2, and associated inverters and drivers. When the receiver is in the local operating mode, the rf gain input voltage, received on board pin C17 from the RF GAIN potentiometer on the front panel, is converted to a binary code for loading into section U1 of the receiver shift register. This code is also converted back to an analog voltage and applied, via board pin C22, to the gain control input of the receiver section. When in the remote operating mode, the gain control data from the receiver register is converted to an analog voltage for controlling the receiver gain.

When the receiver is in the local operating mode, L/R status board-input pin BC is at logic low, which disables NAND gate U23A and enables NOR gate U22A. Inverter U24B converts the L/R status logic low to logic high, which is used to enable NAND gate U23B, turn off transistor Q3, and turn on transistor Q4 via inverter U28F. With Q3 off, CR3 becomes forward biased such that negative voltage is applied to the gate of FET Q1 and turns it off. With Q4 on, positive voltage (+5 V) applied to the cathode of CR4 reverse biases CR4, resulting in

0 V being applied to the gate of FET Q2, turning it on. The positive voltage from the RF GAIN potentiometer (board pin C17) is therefore applied, via X1 non-inverting operational amplifier buffer U30B and FET Q2, directly to the board rf gain output, pin C22. Trimmer-potentiometer R14 is used to match the manual gain control voltage to an equivalent A/D converter-output gain control voltage passed by FET Q1 when in the remote operating mode. The gain control output voltage of U30B is also applied as a reference to the inverting input of comparator U46.

C2-CR2-R2 and C1-CR1-R1 are identical differentiator circuits which produce positive spikes. The $\overline{\text{Load B}}$ output of inverter U24A drives differentiator C1-CR1-R1, and the Load B output of U45D drives differentiator C2-CR2-R2. Therefore, C2-CR2-R2 produces its spike at the beginning of period 2 of the program cycle, on the leading edge of Load B, while C1-CR1-R1 produces its spike on the trailing edge of Load B. Since U23A is, at this point in the description, assumed disabled, the corresponding differentiator output does not reach the parallel-load data strobe input of binary counters U20 and U21. NAND gate U23B, however, passes and inverts the positive spike output of differentiator C1-CR1-R1. U23B and U25C are two-state devices which convert the differentiator spike output to a short (5 μs, approximately), logic low-going pulse, which is applied to the reset inputs of U20 and U21 to reset the counter outputs to zero. Digital-to-analog converter U27 converts the resulting binary zero output from the counter to a zero-current output, which is in turn converted to 0 V by operational amplifier U29B. The output of U29B is applied via X1 inverting operational amplifier U29A to the non-inverting input of comparator U46. Since the comparator's inverting input is positive, the output of the comparator is logic low. This logic low, in being applied to one input of NOR latch U47A-U47B, permits the positive spike from differentiator C1-CR1-R1 to reset the latch output to logic low. This logic low and the L/R status board input logic low permit NOR gate U22A to pass 250 kHz system clock pulses received on board pin C13 from the synthesizer section. The counter begins counting these clock pulses upon termination of the logic low reset pulse, which occurs approximately 5 μs after the trailing edge of the Load B pulse. As the count increases, the D/A converter analog output current increases, causing the output voltage of U29A to correspondingly increase. As the count increases the point will eventually be reached when the output voltage of U29A equals (or rather, very slightly exceeds) the rf gain voltage applied to the inverting input. At this point the output of comparator U46 changes from logic low to logic high, causing the NOR latch to change state. The resulting logic high output from the NOR latch disables NOR gate U22A, thus stopping the counter. Because the counter counted for a period proportional to the rf gain voltage from the front panel potentiometer, the counter's binary code output is numerically proportional to this voltage. This data is parallel-loaded into shift register section U1 on the trailing edge of the first Clock 2 pulse of period 2 in the next program cycle, as previously described. Soon after the data is loaded, the trailing edge of Load B again resets the counter and the NOR latch, thus initiating a new counting cycle.

When the receiver is in the remote operating mode, the L/R status board-input pin BC is at logic high, which enables NAND gate U23A and disables NOR gate U22A. Inverter U24B converts the L/R status logic high to logic low, which is used to disable NAND gate U23B, turn on transistor Q3, and turn off transistor Q4. Q3 and Q4 in turn, turn on FET gating transistor Q1 and turn off FET Q2, thus permitting the D/A converter output to control reciever gain. Since U22A and U23D are disabled, the binary counters do not count and are not reset. However, NAND gate U23A now passes and inverts the positive spike output of differentiator C2-CR2-R2. U23A and U26A are two-state devices which convert the differentiator spike output to a short (5 μs, approximately), logic low-going pulse, which is applied to the parallel-load command (data strobe) inputs of U20 and U21. Therefore, U20 and U21 serve as storage registers which parallel-load the rf gain data from shift register section U1 on the leading edge of the Load B pulse, which occurs at the beginning of period 2 of the program cycle. D/A converter U27 and current-to-voltage converter U29B convert this data to a voltage output which is applied, via inverting X1 operational amplifier U29A and FET switching transistor Q1, to board pin C22 for application to the receiver section gain control input. The gain control data word stored in the counter is also parallel-loaded into shift register section U1 on the trailing edge of the first Clock 2 pulse of period 2, as previously described.

4.5.2.5 Type 791202 Tuning Dial Encoder Assembly (A25). - This assembly converts tuning dial rotation to two square wave outputs of frequency proportional to the rate of rotation, with a phase relation of plus or minus 90°, depending on the direction of rotation. This is achieved by situating two light-emitting diodes (LED) and two photodiodes on either side of a fanlike mechanical chopper which is mechanically coupled to the tuning dial. A pulse occurs on each output line every 3° of rotation. The relative physical positions of the two LED-photodiode pairs with respect to the mechanical chopper produces the lead/lag phase relationship of the output signals.

Refer to the schematic diagram, Figure 7-28. A1CR1 and A1CR2 are the above-mentioned LED's, and A2Q1 and A2Q2 are the respective photodiodes. Transistors A2Q3 and A2Q4 serve as bias-current sources for the LED's, with trimmer potentiometers A2R1 and A2R2 setting the levels. In practice, A2R1 and A2R2 are used to set the pulse output levels of the photodiodes, which is possible because light intensity from an LED is a function of bias current. The two square wave outputs from pins E5 and E6 of optical receiver board A2 are applied to schmitt trigger circuits on the front panel register board (A22).

4.5.2.6 Type 791276 Optional Tuning Connector Filter (A24). - Figure 7-27 is the schematic for this circuit. The optional tuning connector filter contains three lowpass LC filters which eliminate noise on the optional tuning input and dc supply output lines connected to the front-panel OPTIONAL TUNING connector. The filtered tuning lines are connected to the tuning dial sense circuit on the Front Panel Register board (A22).

4.5.2.7 Type 791126 Numerical Display/Buffer (A23). - Figure 7-26 is the schematic for A23. The BCD tuned frequency outputs from the front panel shift register board are applied to the numeric indicators (A1U1 through A1U7) via buffers U1 through U5. +5 V for the decimal point is also obtained from the front panel register board, through a 270-ohm resistor. The numeric indicators have built-in storage, and are updated at the beginning of period 3 of the program cycle by the EOC pulse received from the program sequencer board (A20). The EOC input is applied to pin 5 of each indicator.

4.5.2.8 Type 791200-1, -2 Synchronous I/O Module (A16). - The I/O module provides interfacing between the digital control section of the receiver and the remote control unit. This board contains address, data, trigger, monitor, clock, and status line receivers and line drivers, as well as logic circuitry which coordinates these inputs and outputs with operation of the digital control section of the receiver. Figure 7-18 is the schematic diagram for the synchronous I/O module.

U1A, U2A, and U2B are line receivers which receive address, trigger, and serial data from the remote control unit, and U8 and U9 are programmable dual line drivers which provide monitor and command clock, monitor serial data, and local/remote status outputs to the remote computer. Line receiver input impedances are approximately 170 ohms thorugh 0.01 μF capacitance, differential. Input voltages can be as high as $\pm$ 20 V maximum. Differential threshold voltage is between $\pm$ 0.5 V and $\pm$ 1 V, depending on the common-mode voltage. Line driver outputs are differential TTL pairs, shortcircuit proof. Both sides of the output of a line driver are zero when the driver is disabled. Differential output impedances of the line drivers are approximately 360 ohms, as determined by the 180-ohm line-impedance matching resistors in series with the + and - outputs. The remote status line-driver output may not be wired to the rear-panel connector in earlier models of the WJ-8888.

The output of the data input line receiver (U2B) is routed via board pin Y directly to the multiplexer on the front panel register board (A22). The other board outputs are controlled by logic gates, however, except the remote request output in the standard WJ-8888. In this case jumper JW2 is not connected and the remote pushbutton input (board pin 11) is simply routed through U5C and U7C to the program sequencer board (A20) via board pin 10. Control of NOR gate U5C when jumper JW2 is connected (and JW1 is not connected) is described below. When no address is received from the remote control unit, the output of line receiver U1A is high. Also, in normal operation, the power fail latch input (board pin 12) is low, enabling NOR gate U5B such that the U1A logic high output is gated through to result in a logic high being presented to the set (pin 8) input of data-type flip-flop MV U4B. This logic high sets the Q output of U4B at logic high and the $\overline{Q}$ output at logic low, thus disabling all of the remaining board outputs by disabling the gates connected to the Q and $\overline{Q}$ outputs of U4B. Upon reception of an address from the remote control unit, the output of U1A goes low, which results in the removal of the logic-high set input to U4B. The outputs of U4B do not change until commanded by the EOC pulse (received on

board pin E) at the beginning of period 3 of the program cycle. This prevents interruption of an ongoing program cycle. On occurrence of the EOC pulse, which is applied to the clock input of U4B, the logic low output of U1A is gated through U4B to the Q output, and the complementary $\overline{Q}$ output of goes high, thus enabling NOR gate U5A, the remote status section of line driver U9, and NAND gates U6A and U6B. During period 2 of the next program cycle, $\overline{2}$ received on board pin 15 and gated through U5A enables both sections of line driver U8, such that Clock 1 (received on board pin B) and the data word clocked out of the receiver register and on to the data node (and received on board pin D) are applied to the remote control unit during period 2 of the program cycle. When the remote status section of line driver U9 is enabled, its output is a function of the board local/remote status input (board pin 16) from the program sequencer board (A20).

When power fails the board power-fail latch input (pin 12) goes high, reverse biasing CR1 to permit +5 V to be applied to U5B to disable the gate for as long as the +5 V supply voltage holds up. (The P. F. latch input is powered by the battery. Diode CR1 prevents drain on the battery when the +5 V supply drops out on power failure.) When U5B is thus disabled, the set input (pin 8) of U4B goes high, terminating a present address or preventing an address from being received from the remote control unit. This prevents possible garbled data from being applied to the remote control unit in the early stages of power failure when reduced supply voltage is causing irregular operation of the receiver circuitry. The reverse action occurs when the power comes back up. That is, the PF latch input remains high until the +5 V supply is fully recovered, ensuring that garbled data is not applied to the remote control unit during intermediate and later stages of recovery.

The output of NAND gate U6A is applied to the enable input of the command clock section of line driver U9. This gate therefore permits Clock 3 to be applied to the remote control unit, via the command clock section of line driver U9, when, simultaneously, the L/R status board input is high (indicating that the remote mode is active), the multiplexer address, received on board pins V and W from the program sequencer board, is 11 (indicating that the multiplexer is receptive to the remote data output from pin Y of this board), and the address input is gated through U4B as described above. Since Clock 3 is disabled in periods 3 and 4 of the program cycle (see basic timing diagram), the first command clock occurs at the beginning of period 1 of the program cycle, and because the multiplexer address changes (to 00) at the beginning of period 2, the command clock is terminated at the end of period 1 of the program cycle.

The output of NAND gate U6B is applied to the remote trigger input of the program sequencer board. The remote trigger board input (pins 21 and 20) from the remote control unit is therefore able to initiate a remote-active sub-mode only when, simultaneously, the L/R status board input is high (indicating that the remote mode is active) and the address input is gated through U4B as described above. Note from previous descriptions of the program sequencer circuitry that the mux address becomes 11 only when commanded by the remote trigger; therefore, NAND gate U6A does not permit the command clock to be applied to the remote control unit unless a remote trigger is received.

In the WJ-8888-5, jumper JW1 is not connected and JW2 is connected. Therefore, +5 V applied to U6B via R11 permits U6B to be operated by the remote trigger and address inputs, independently of the status input. With JW2 connected the OR function provided by U5C and U7C permits the board remote request output (pin 10) to be activated by the remote trigger or by the REMOTE pushbutton on the front panel. That is, reception of a remote trigger causes the receiver to change to the remote operating mode regardless of the present manually selected operating mode of the receiver.

4.6 POWER SUPPLY SECTION

4.6.1 PRIMARY POWER. - Refer to the chassis wiring schematic, Figure 7-33. The power supply section is shown in the upper left-hand corner of the schematic. The ac line voltage from plug FL1P1 is filtered for transients and high frequency noise by line filter FL1 before application to step-down transformer T1. The ac power switch, S1, is connected in series with one side of the ac line. Ferrite beads (FB6 through FB9) eliminate power line transients caused by power switch operation. Line-voltage selector switch S2 connectes the ac input line to appropriate primary windings of T1 for 220 V or 115 V operation. The windings are connected in parallel for 115 V operation. Series connection of the windings for 220 V operation produces a greater transformer step-down ratio. Line fuse F2 provides protection when operating from 220 V, while fuse F1 provides protection primarily for 115 V operation.

One secondary winding of the transformer operates the blower motor; the outputs from the remaining windings operate dc power supplies. Full-wave-connected rectifier diodes CR1 and CR2 and filter capacitors C100 and C101 provide unregulated +10 V for operating the +5 V supply on board A27, for illuminating the front panel meter lamps on board A29 and the AC POWER pushbutton switch lamp, and for operating the pushbutton lighting circuit on switch encoder board A21. The four regulated supplies are contained on boards A26 and A27.

4.6.2 POWER SUPPLY BOARD SCHEMATIC DESCRIPTIONS. - The two power supply boards produce regulated ± 5 V dc and ± 15 V dc which operate the majority of the circuitry in the WJ-8888. Three of the supplies employ conventional regulating circuitry, while the +5 V supply utilizes a regulator which operates in the switching mode to permit relatively small size components to produce high power output at high efficiency.

4.6.2.1 Type 76210-7 ± 15 V Power Supply Board. - Refer to the schematic, Figure 7-29. The two 15 V power supplies on this board are identical, except that opposite polarity outputs are taken. Full-wave rectifiers U1 and U3 convert the 25 V ac from two windings of power transformer T1 (on chassis) to + and -22 V dc. Chassis-mounted filter capacitors C97 and C98 provide initial filtering of the outputs of rectifiers U3 and U1, respectively. The unregulated dc output from U1 is applied to the +15 V regulator comprising Q1 and U2, and the unregulated dc outut from U3 is applied to the -15 V regulator comprising Q2 and U4. Regulator integrated circuits U2 and U4 are each essentially composed of a temperature-

compensated reference amplifier, error amplifier, series pass transistor, and current limit circuitry. The outputs of U2 and U4 control series pass transistors Q1 and Q2, and the regulated dc outputs of these pass transistors are, in turn, applied to the power-supply loads (receiver circuitry) through chassis-mounted current-sense resistors R1 and R2. Board pins 13 and 11 are +15 V and -15 V supply output tie-points which return current reference and voltage sense inputs to integrated-circuit regulators U2 and U4. Pin 2 of the regulator IC's are the current-limit sense inputs. Voltage-sense divider potentiometers R2 and R5 permit fine adjustment of the regulated output voltages.

4.6.2.2 Type 76209 ±5 V Power Supply Board. - The schematic for this board is Figure 7-30. The board contains a conventional -5 V regulated power supply and a +5 V "switching regulator" circuit. Diode module U1 provides full-wave rectification of the low voltage output of one winding of chassis-mounted transformer T1. The rectified voltage is smoothed by chassis-mounted capacitor C99 before application to the collector of Q1 and reference circuit R1, R2, C2, and VR1. Q1 serves as an emitter-follower pass transistor referenced by 5.6 V reference diode CR1. Since the emitter voltage of a forward-biased diode is fixed at 0.6 V less than the base voltage, the output of the supply is -5 V less the small voltage drop across 1-ohm resistor R9 due to load current. R9, CR2, and CR3 form a protective current limiting circuit for the -5 V supply. CR3 is a conventional silicon diode and CR2 is a hot-carrier diode, having fully-on forward drops of 0.6 V, and 0.4 V, respectively. The two diodes in series are in parallel with the series combination of R9 and the emitter junction of Q1. As long as the current drain on the supply is less than 0.4 A, CR2 and CR3 are not fully forward biased and do not significantly affect operation of the supply. When the current drain on the supply exceeds 0.4 A, the voltage across R9 exceeds 0.4 V. Since the maximum forward voltage drop of the diode combination is 1.0 V, it follows that the emitter junction drop of Q1 must fall below 0.6 V, starving Q1 such that the supply current is limited at 0.4 A.

The +5 V switching regulator is composed of referenced amplifier U2, transistors Q2 and Q3, "free-wheeling" diode CR1, and associated passive components. The lowpass LC filter composed of L1, C3, C1, C6, C9, and C10 isolates the regulator from the +10 V unregulated dc input line to prevent high-frequency switching components from getting back into the ac input line and the other power supplies. The output of the filter is applied to the collector of series switching transistors Q2, the emitter of driver transistor Q3, and the power input pin of referenced ampifier U2. Transistor Q2 functions as a switch in series with an output filter which produces a voltage proportional to the duty cycle (time on/total time) of the transistor. The output filter consists of two L sections comprising L3-C8 and L2-C5. "Free-wheeling" diode CR1 provides a current path for the reactive current produced by the collapsing magnetic field of inductor L2 when Q2 turns off. Referenced amplifier U2 is connected such that the circuit self-oscillates at approximately 24 kHz, with a duty cycle determined by the value of the dc output voltage referenced to a precision voltage source internal to U2.

The internal U2 reference voltage is, in effect, connected to the non-inverting amplifier input (pin 5) through a resistance which is small compared to R4. This internal resistance and R4 form a voltage divider which permits large variations of the output voltage of Q2 (+10 V with Q2 on, 0.6 V with Q2 off and CR1 conducting) to cause small variations (hysteresis) of the effective reference voltage applied to the non-inverting input of the amplifier. An output voltage sample is obtained from the mid-point of the output filter via output-voltage-adjust potentiometer R7, and applied to the inverting input (pin 6) of U2.

Upon turn-on of the power supply the inverting input of U2 is 0 V and the non-inverting input voltage is pulled down only slightly from the reference voltage to the lower hysteresis point. Therefore, the output of U2 is high and causes driver transistor Q3 to turn Q2 fully on. This causes the inverting input of U2 to begin increasing toward the reference voltage at a rate limited by the inductance of L2. The non-inverting input voltage increases to the upper hysteresis point when Q2 turns on. When the inverting input voltage equals (or rather very slightly exceeds) the non-inverting voltage, U2 changes state and turns Q3 and Q2 off. CR1 conducts and the non-inverting input voltage of U2 drops to the lower hysteresis point, and the inverting input voltage begins to drop as the field of L2 collapses. When this voltage equals (or rather is very slightly less than) the non-inverting input, U2 again changes state and turns Q2 on. The non-inverting input voltage reverts to the upper hysteresis point, the inverting input voltage begins to increase toward this voltage, and the process continues at a 24 kHz rate. Since the ratio of R4 to the internal reference source resistance is very large, permitting only very small variations in the effective reference voltage at the non-inverting amplifier input, and the inverting input voltage need vary only by this amount, the 24 kHz ripple at TP1 is small and easily eliminated by the remaining stage of the output filter. The frequency of oscillation is determined by the build up and collapse times of the divided-down voltage of L2 (inverting input of U2) with respect to the upper and lower hysteresis points of U2. If the inverting input voltage of U2 falls outside of the range between the two hysteresis points, action similar to that described above for turn-on will bring the voltage back into range.